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ELECTRONIC DESIGN

DECEMBER 2, 1993

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

22 FEB 1994

CHIP SET ADDS VOICE TO DATA/FAX MODEMS

- SPECIAL REPORT: PROGRESS IN ELECTRONIC-SYSTEMS DESIGN AUTOMATION
- TEST & MEASUREMENT UPDATE: WHAT'S NEW IN FUNCTION GENERATORS
- VERSATILE PLDs AIM AT COMPLEX LOGIC
- IEDM PREVIEW
- PEASE PORRIDGE

T. Vitolo

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DETECTION SYSTEMS P L 34994

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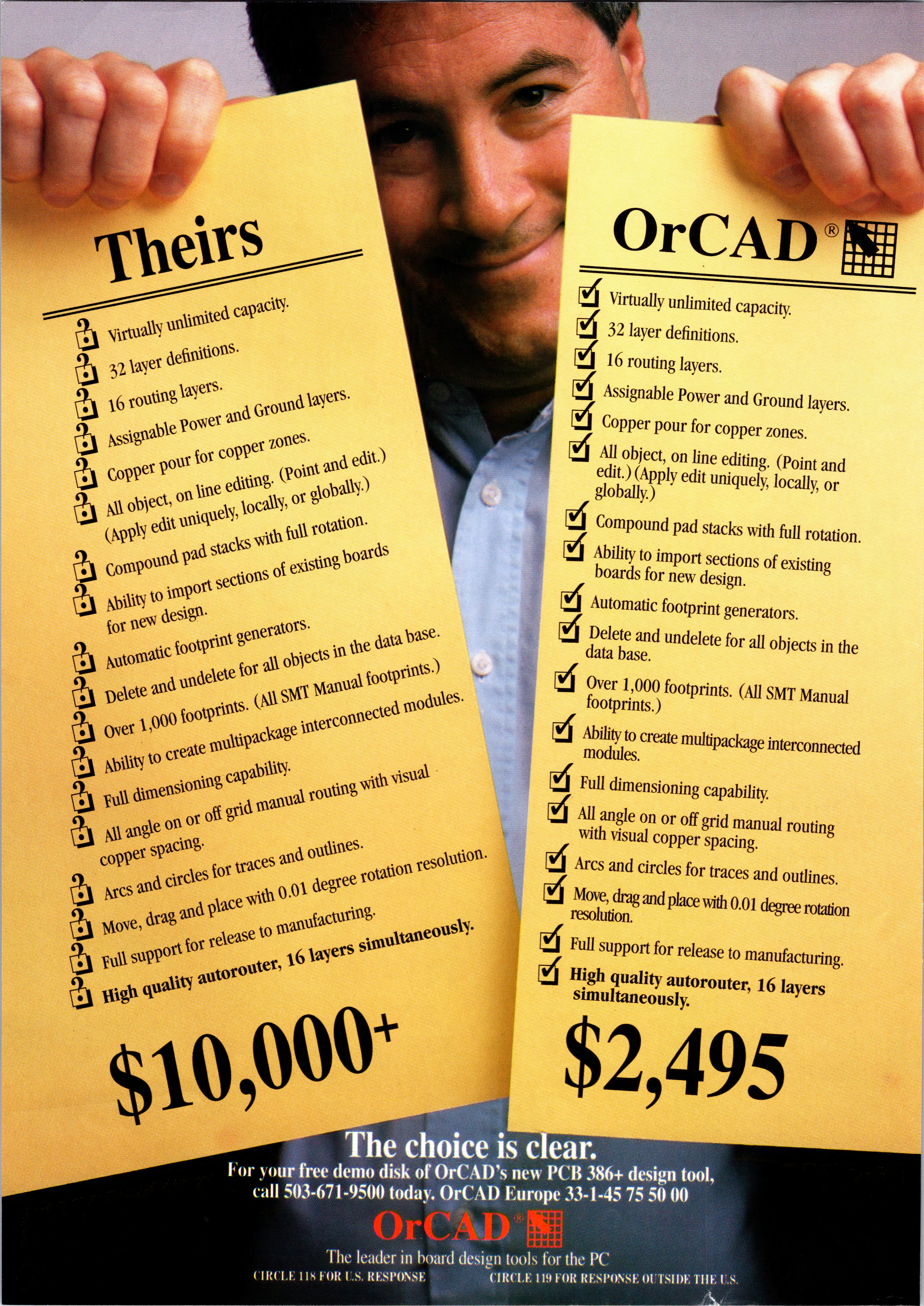

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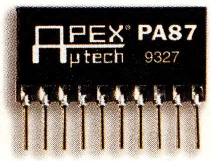

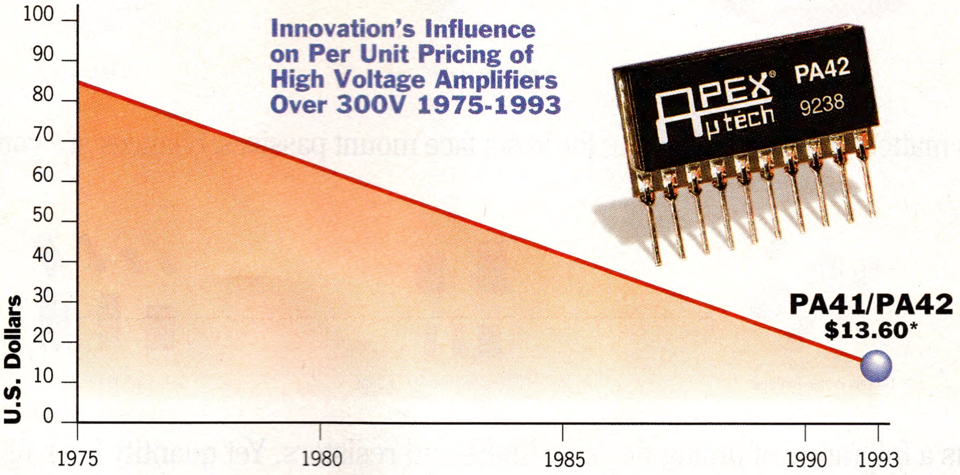

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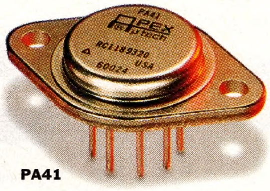

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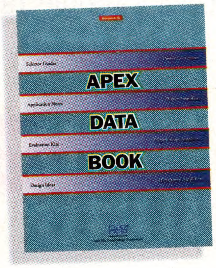

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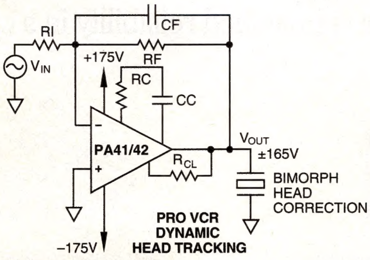
Information on the PA41, PA42 and the PA87 is included in the new 6th edition Apex DC/DC Converter, HV and Power Amplifiers data book. Call today for your free copy. **1-800-862-1021**.



PRODUCT SPECIFICATIONS

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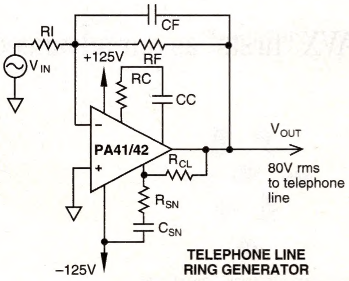
PA87	100V-450V	200/300	3mA	7.5W	$52.00



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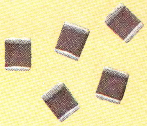
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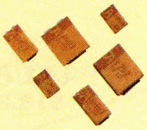
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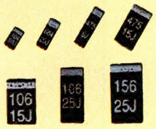

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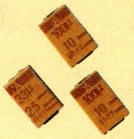
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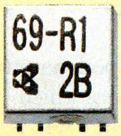
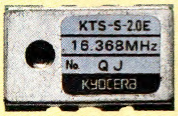
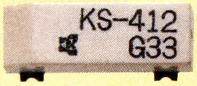


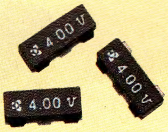
EK Series-Voltage Controlled Oscillator



KTS Series-Temperature Compensated Crystal Oscillator



KS Series-Crystal



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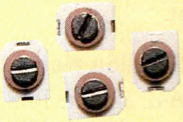
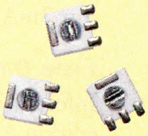

CTZ Series-Trimmer Capacitors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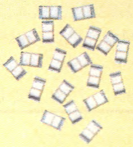
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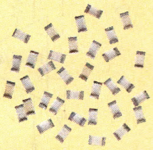
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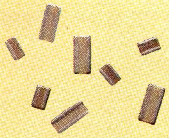
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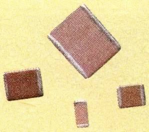
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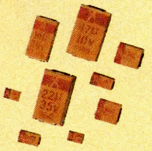
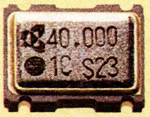

TAJ Molded Ta Caps

AVX TIMING DEVICES

AMO Series-Clock Oscillator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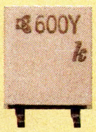
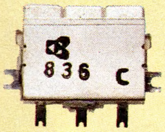

KBR-Y Series-KHz Resonator

AVX FILTERS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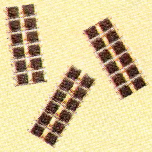
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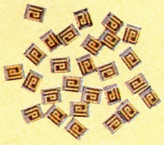
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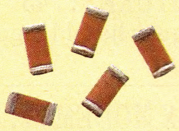
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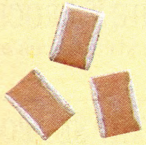
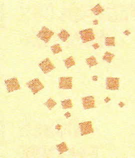

High-Voltage MLC Caps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Quicklook

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ELECTRONIC DESIGN 40 YEARS AGO

SWAC Improvements

SWAC, the National Bureau of Standards' Western Automatic Computer, is now operating 120 hours a week on complex problems in physics, engineering, mathematics, statistics, and meteorology. About 3/4 of this time is devoted to problem solution, while the remainder is used for maintenance, engineering development, and new equipment tests.

Constructed in 1950 by the National Bureau of Standards, Washington, D.C., under the sponsorship of the Wright Air Development Center, SWAC is the first of the high-speed electronic computers to be completed with the fast Williams cathode-ray tube memory and operates at a rate of 16,000 additions or 2600 multiplications per second. Through the installation of a magnetic drum auxiliary memory, the scope and complexity of the problems handled by the machine have been greatly extended. The new memory holds 16 times as much mathematical information as the cathode-ray tube memory, with which it will be used to increase the overall memory capacity of the machine.

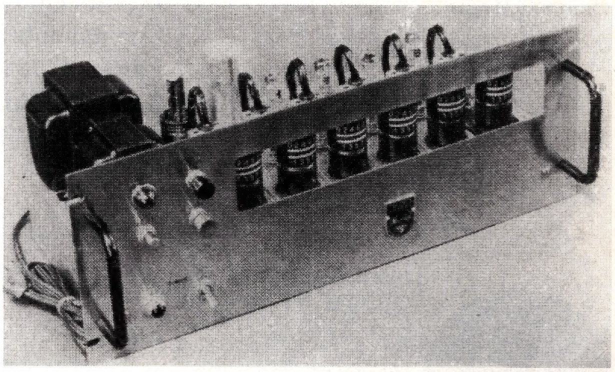
SWAC contains about 2600 tubes and 3700 crystal diodes, and the average tube life is between 8000 and 1000 hrs. To date, few tubes have been lost because of heater failure. The largest percentage of tube failures have resulted from low emission and intermittent shorts. All electronic components in the computer are mounted on a removable plug-in chassis, so that faulty operation can usually be corrected by replacing a bad chassis with a spare. An air conditioning unit was installed to maintain the incoming air in the ventilation system at a constant temperature. This minimized temperature cycling of crystal diodes and decreased their failure substantially.

Operating efficiency has been increased by a loudspeaker and buffer tube with a plug-in arrangement which allows the operator to listen to the commands in a problem (e.g. an alternate succession of add and subtract commands produces an 8kc note). The addition of one tube and a few crystals created a converting output command, effective only with the output typewriter and tape punch, which converts fractional binary numbers to octal, decimal, or any other base up to 16.*(Electronic Design, December 1953, p. 6.)*

This is a fascinating item, filled with comments on the features and characteristics of early computers: a Williams tube, magnetic drum memory, tube reliability, the use of air conditioning, a choice of output radix, and even installing a loudspeaker to listen to the computer as it performs its operations. Have you listened to your computer's logic circuits lately?—Ed.

Decade Scaler Has 30,000 Events/Sec Rates

This high-speed six-digit Decade Scaler is adapted for use in telecommunication and in computers for frequency and nuclear measurements. Including a power supply and appropriate control circuits, it has a maximum cyclic rate of 30,000 events per sec, minimum resolving time of 25msec, and a total registration of 999,999. Direct indicating Type E1T tubes are used, and the input circuit is not limited to any specific wave shape. The instrument is designed for standard rack mounting. Research & Control Instruments Div., North American Philips Co., Inc., 750 S. Fulton Av., Mt. Vernon, N.Y. *(Electronic Design, December 1953, p. 35.)*



Regular readers will recall the Amperex E1T decade-counter tubes in our July 22 "40 Years Ago" column. Apparently, this is one of its first applications.—Ed.

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Herb Baum, Pres., Campbell North & South America and Chm. of the Advertising Council.

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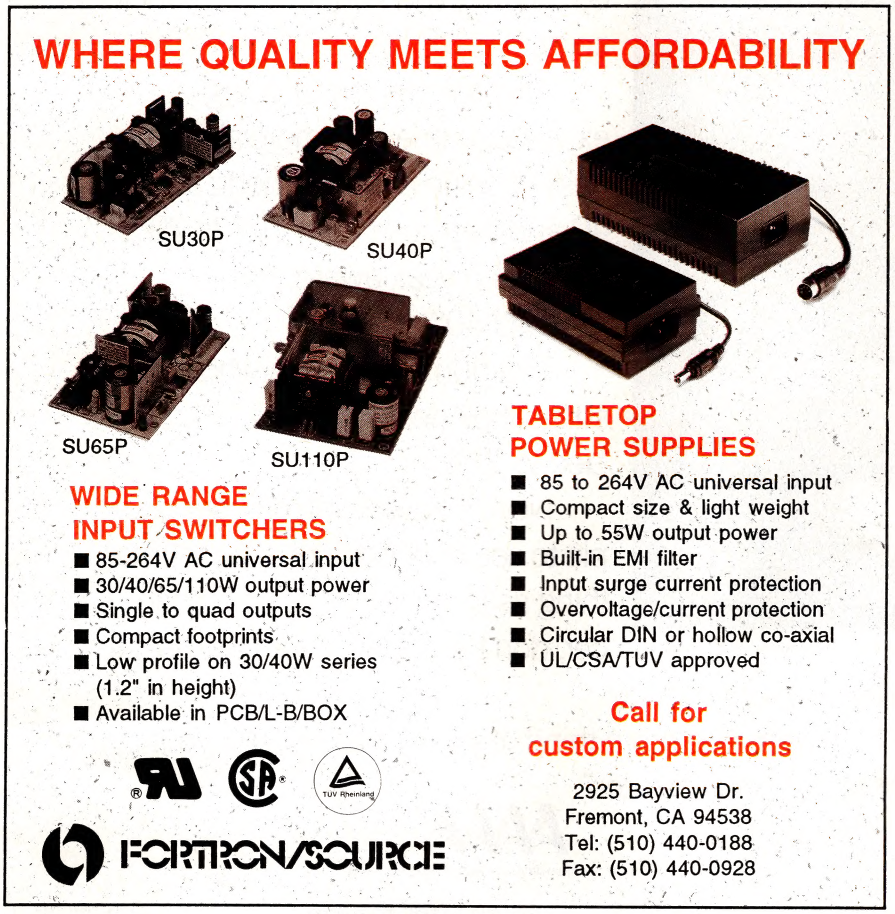

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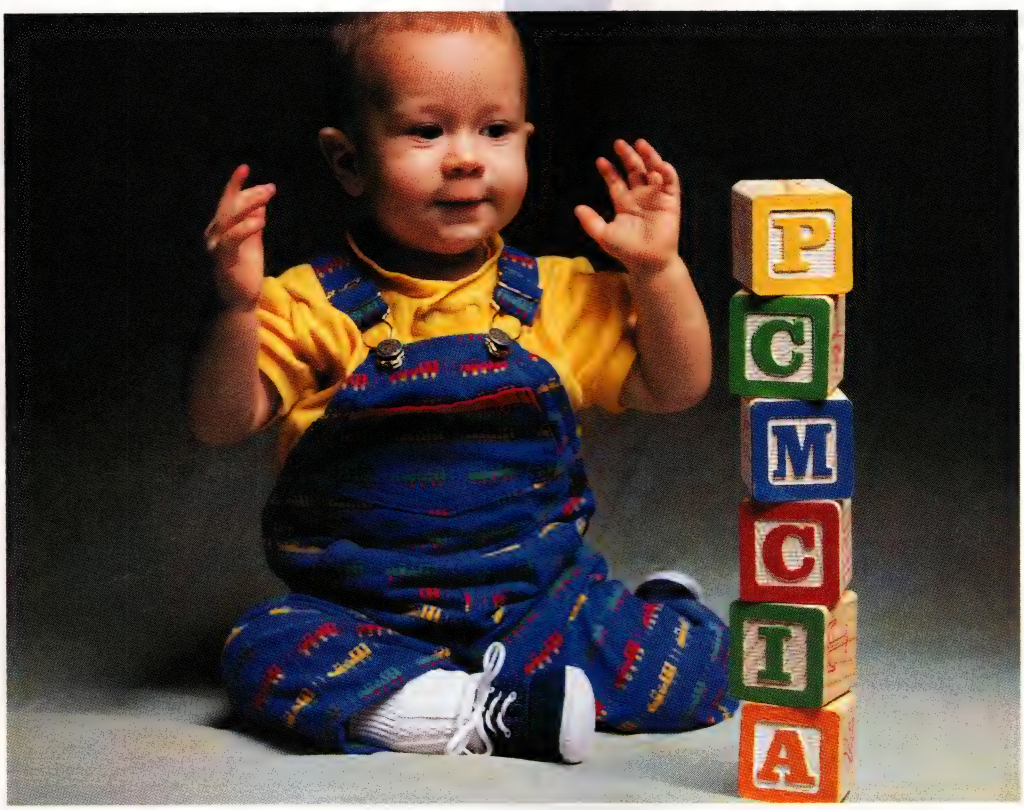

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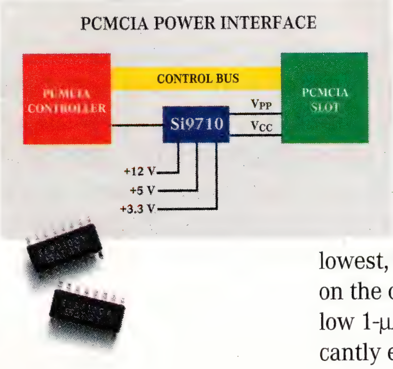

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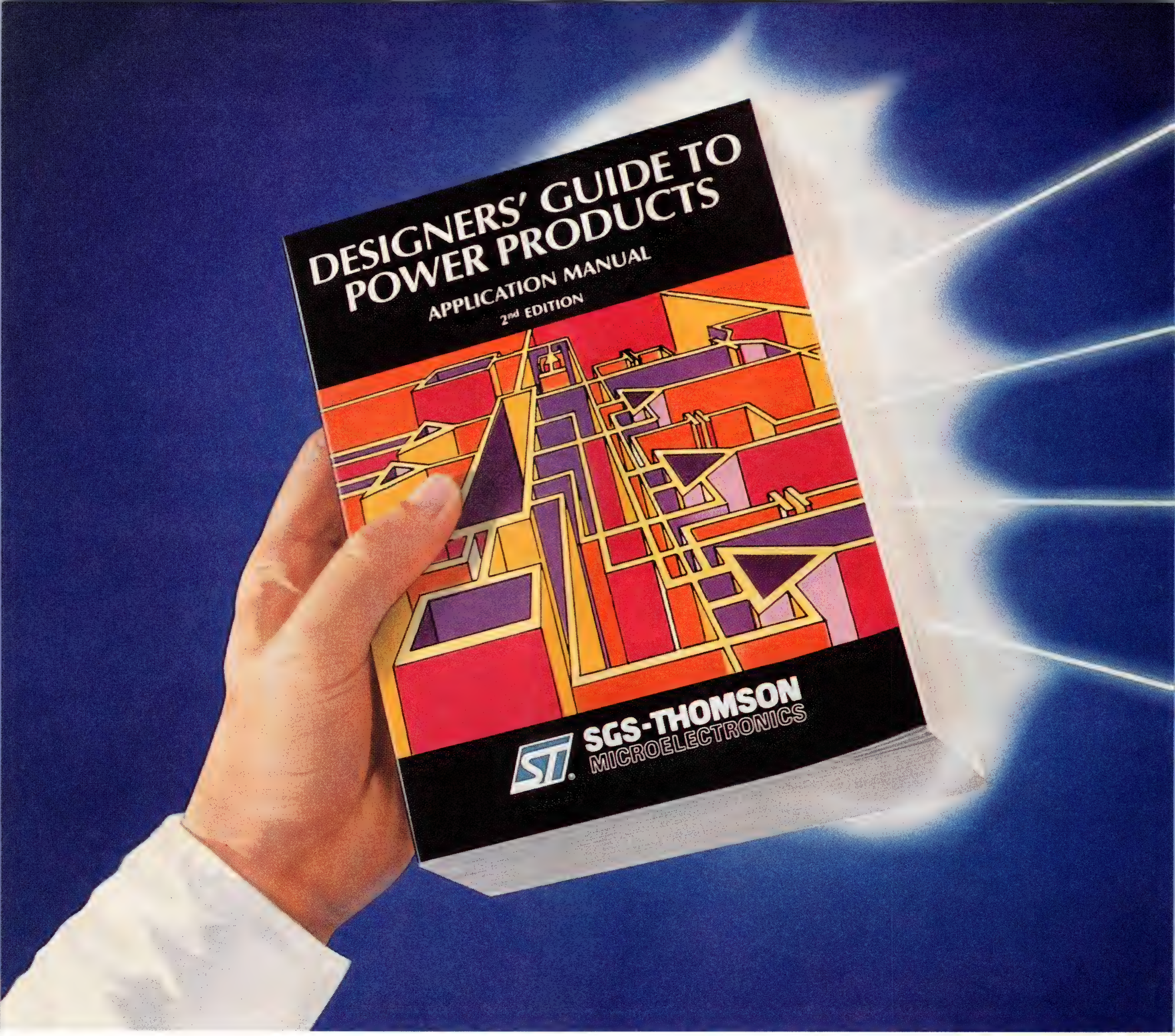

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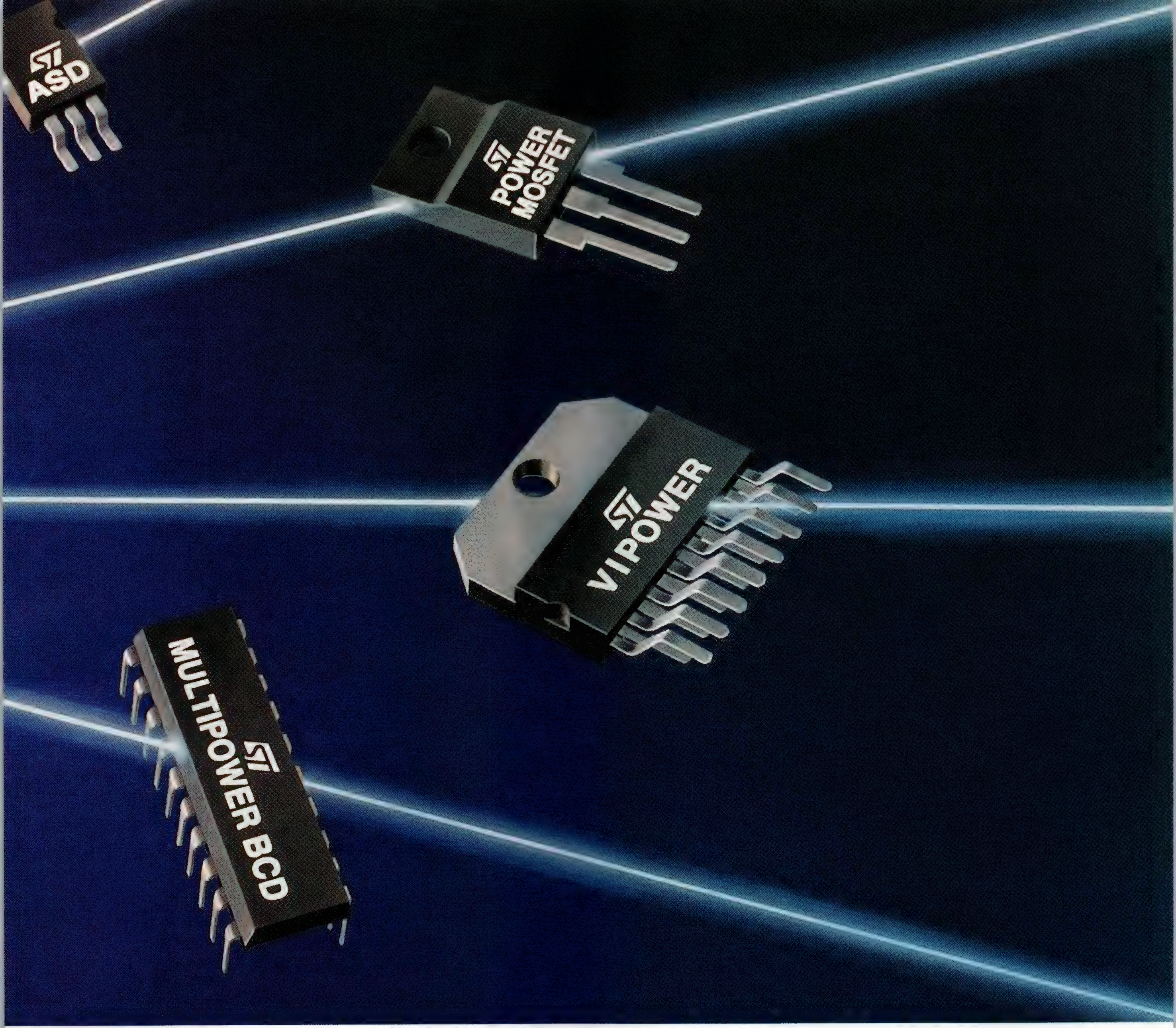

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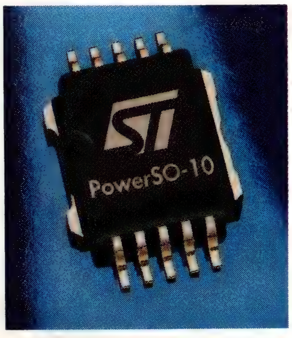

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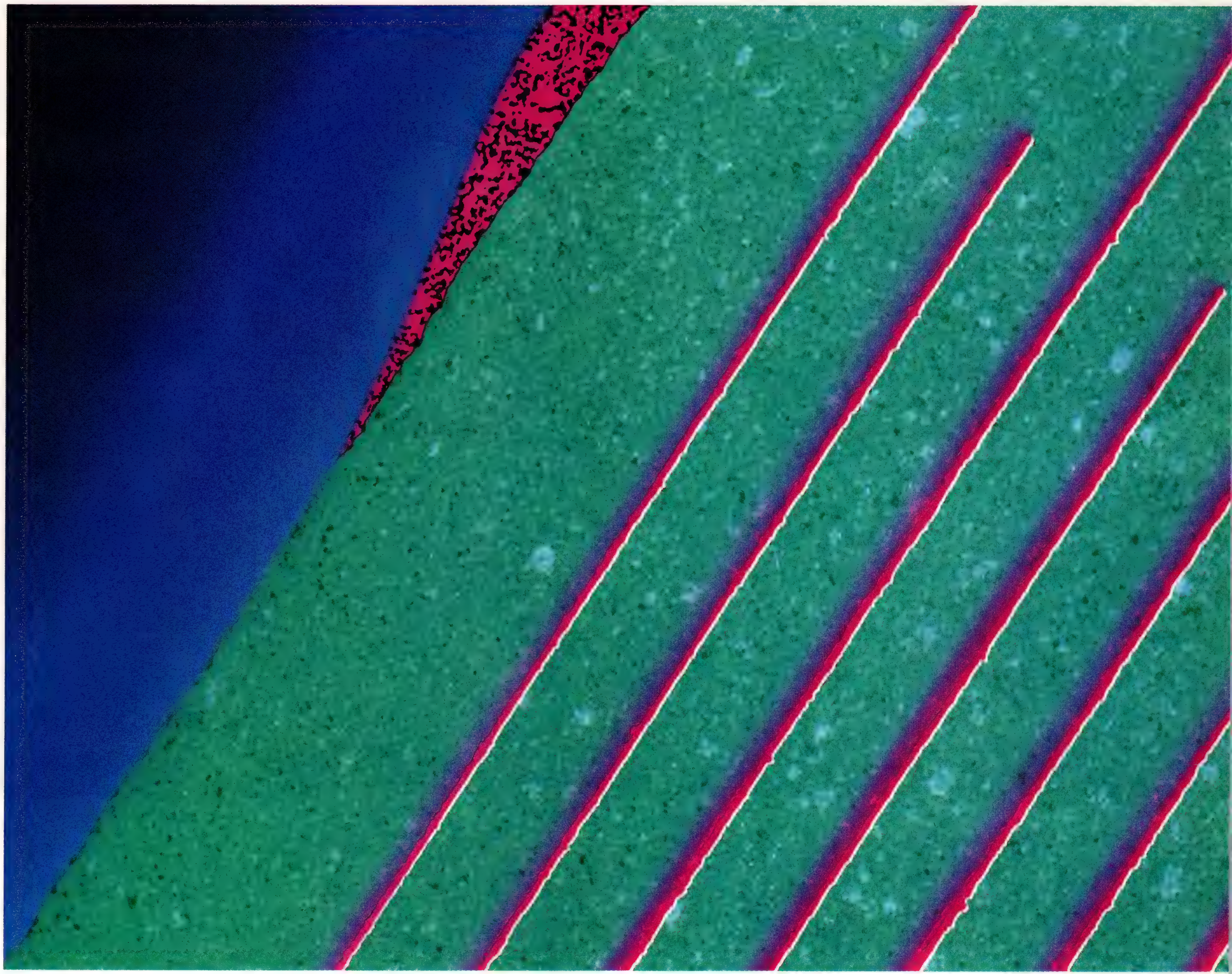

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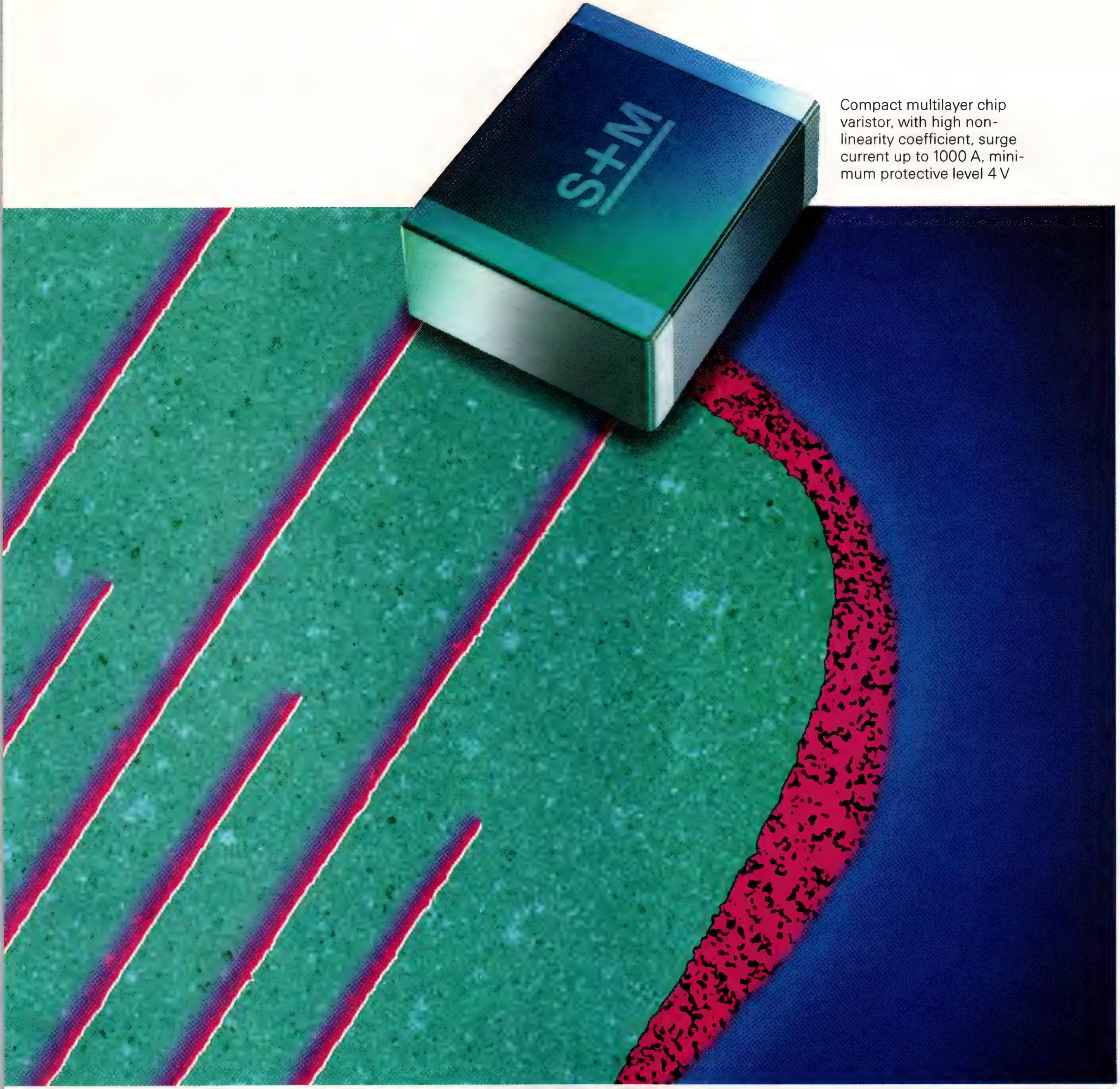

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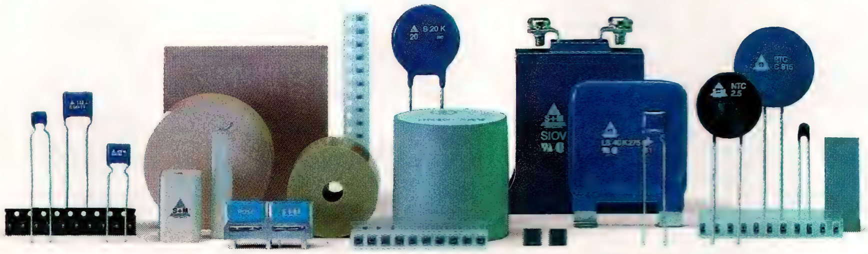

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CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.

EDITORIAL

FROM HAND CRANKS TO SATELLITES

In our Nov. 1 issue, we published letters from readers who responded to the "40 Years Ago" item concerning a 56-lb. hand-cranked lifeboat radio. Several readers recognized it as the "Gibson Girl" emergency radio, so called because of its hourglass shape, and reminisced about their experiences with the radio (if you missed those colorful letters, see p. 127 of the Nov. 1 issue). The story, however, has yet another footnote: We recently received a letter from Jack G. Ganssle, president of Softaid, Columbia, Md., who wrote:

"I couldn't resist responding to the comments made about the 56-pound 'Gibson Girl' lifeboat transmitter from so many years ago. Times have certainly changed. In 1992, while racing alone across the Atlantic, I had to abandon ship 500 miles from land after 32 days at sea. I activated a modern 406-MHz EPIRB [Emergency Position Indicating Radio Beacon] transmitter that sent a personal ID to one of six orbiting satellites. The spacecraft computed my position via Doppler shift and downlinked the data to the Coast Guard, who vectored a German container ship to my rescue. Elapsed time: 4 hours from turning the unit on till the ship was in sight!"

A letter such as this really exemplifies the tremendous gains made in electronics technology over the past 40 years. More specifically, though, it highlights one of today's major market and technology trends—the growth of wireless technology. While it's fascinating to compare today's VLSI-based portable devices with the 50-lb. behemoths of yesteryear, it's much more exciting to think about the future of wireless technology, which is arguably the fastest-changing, fastest-growing segment of the electronics industry.

Many individual technologies are converging on the wireless market, spurred on by recent FCC actions to open up new frequencies and by rapid consumer acceptance of portable communications devices. We're seeing improvements in RF semiconductor devices on many fronts, as well as lower-cost 16- and 32-bit microcontrollers to control the functions of wireless units, and more efficient battery power-control ICs for portable applications. In addition, major competitive battles are shaping up among the cellular and digital radio service providers. The exploding technology has also compelled some companies to expand their efforts to participate this market. For instance, Analog Devices, a major supplier of linear ICs, data converters, and digital signal processors, recently established an RF division to pursue the wireless market.

With such activity, my guess is that in the next 5 to 10 years, wireless technology will advance as far beyond the emergency radio beacon-satellite system of Mr. Ganssle's boat as that beacon is beyond the hand-cranked Gibson Girl radio.

Steve Scrupski

Editor-in-Chief

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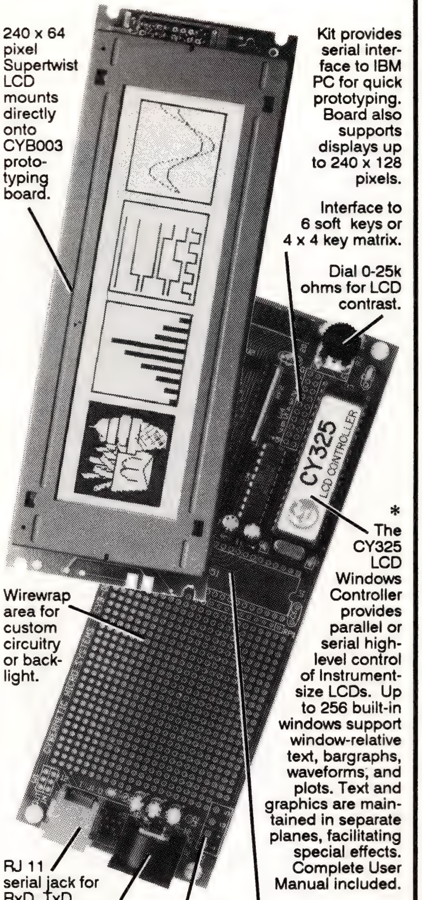

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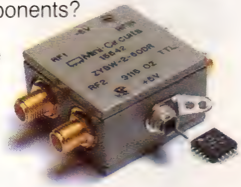

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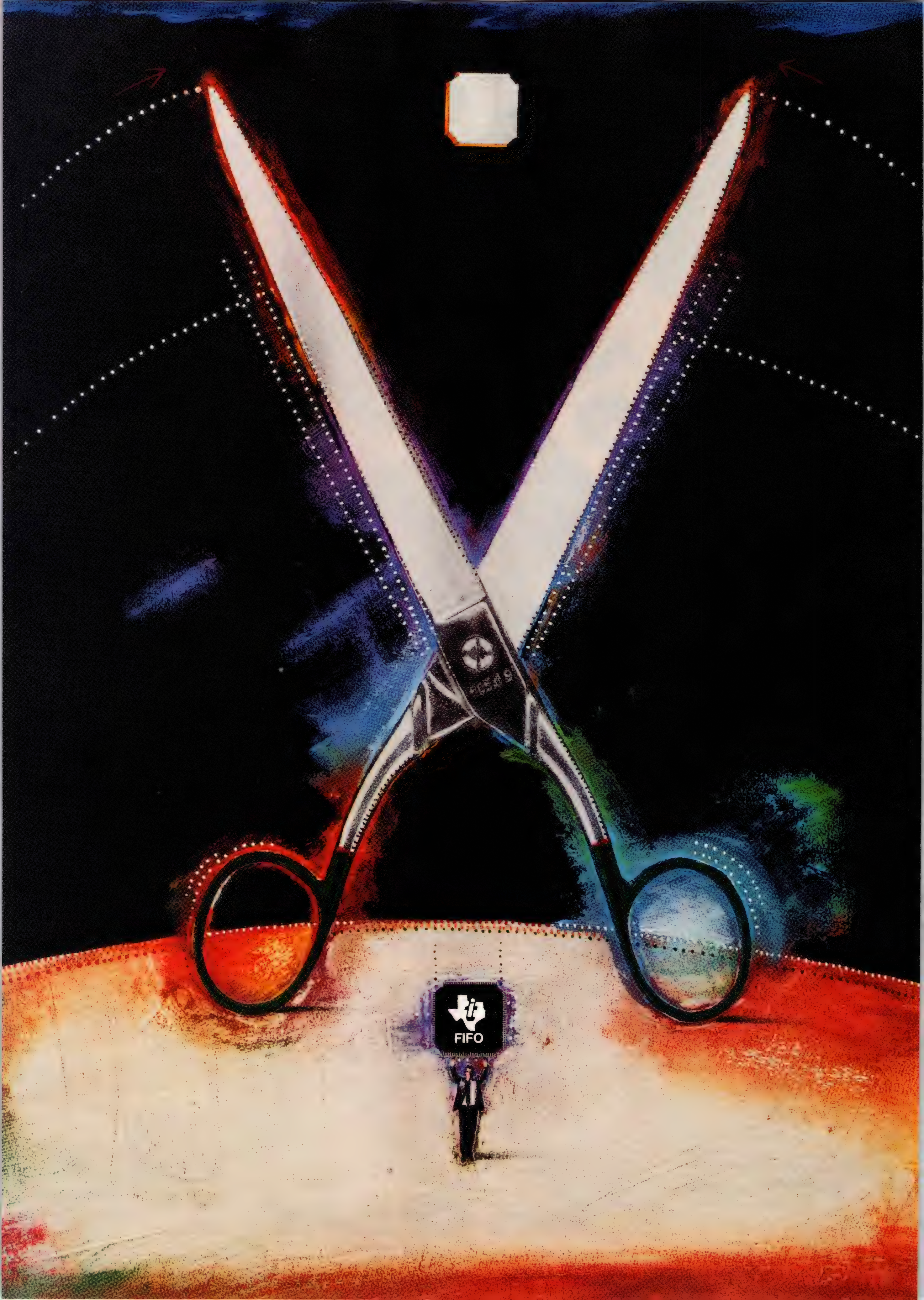

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CIRCLE 98 FOR U.S. RESPONSE
CIRCLE 99 FOR RESPONSE OUTSIDE THE U.S.

DRIVING VXI TO ITS FULL POTENTIAL

The VXIbus standard is a success. But just how successful depends on whom you ask. OEMs are using more and more VXI (VME Extensions for Instrumentation) modules in discrete boxes as well as ATE systems. Among end users, however, VXI's popularity has lagged somewhat. Although VXI modules meet the standard's original intent of offering interoperability between numerous manufacturers, integrating modules from different vendors is more difficult a task than most end users want to tackle. A large part of the problem revolves around software.

Riding to the rescue of prospective VXI users is the VXIplug&play Systems Alliance, which is dedicated to increasing ease of use for multivendor VXI systems users. The group's charter is to endorse and implement common standards and practices in hardware and software that are beyond the scope of the actual VXIbus specifications. To do so, the Alliance will create both formal and de facto standards that define complete system frameworks. The ultimate goal is true "plug-and-play" interoperability at both the hardware and system-software level.

JOHN NOVELLINO
TEST & MEASUREMENT

"The bottom line is that users have been telling us they want more progress in the software area," says Ron Wolfe, VXI marketing manager at National Instruments. "Users expect better cooperation between vendors on the software side. They expect to get software with an instrument. And they expect it to be open and usable in any way they want to use it."

Wolfe notes that a number of instrument driver libraries have been around for some time. But the drivers, usually written by third parties, don't employ the same methodologies, and drivers from one package may not work with drivers from another library. The Alliance feels instrument vendors should commit to writing their own drivers. Although it will not try to standardize the capability of all drivers, the group wants to ensure a common underlying framework for driver development. The goal is to have all drivers work with any software.

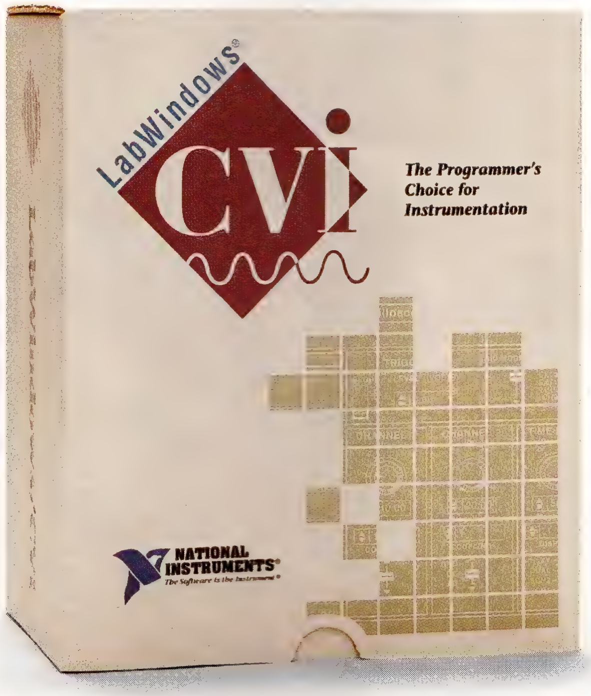
The founders of the Alliance include three of the five founders of the VXIbus Consortium, which wrote the VXI specification and continues to administer it. These include Racal-Dana Instruments, Irvine, Calif.; Tektronix Inc., Wilsonville, Ore.; and Wavetek Corp., San Diego (another was Colorado Data Systems, since bought by Tektronix). The other two Alliance founders are GenRad Inc., Concord, Mass., and National Instruments Corp., Austin, Texas.

Alliance members consider their group to be a "natural complement" to the Consortium. They point out that the Consortium's job is to specify a broad range of baseline technology, not to discuss end-user needs, system software, customer service, technical support, or actual applications. Neither does the Consortium discuss, endorse, or direct product implementation philosophies.

Conspicuously absent from the founders list, however, is Hewlett-Packard Co., the fifth founding member of the Consortium. HP said it wasn't contacted prior to the announcement of the formation of the Alliance. Larry DesJardin, R&D manager for HP's VXI Systems Div., Loveland, Colo., reaffirmed the company's support for open standards in both hardware and software, citing its efforts in VXI, the Standard Commands for Programmable Instruments, and the Standard Instrument Control Language. "It is unfortunate that the Alliance members chose to exclude HP, Radisys, and other major VXI vendors from its formation, but this will not change our historic commitment to support truly open standards," says DesJardin.

There's bound to be some political problems when competing companies with disparate interests try to work on a project of this complexity. But the success of the VXI Consortium proved that these problems can be overcome. For the sake of VXI end-users, let's hope they can be worked out again.

Building Permit.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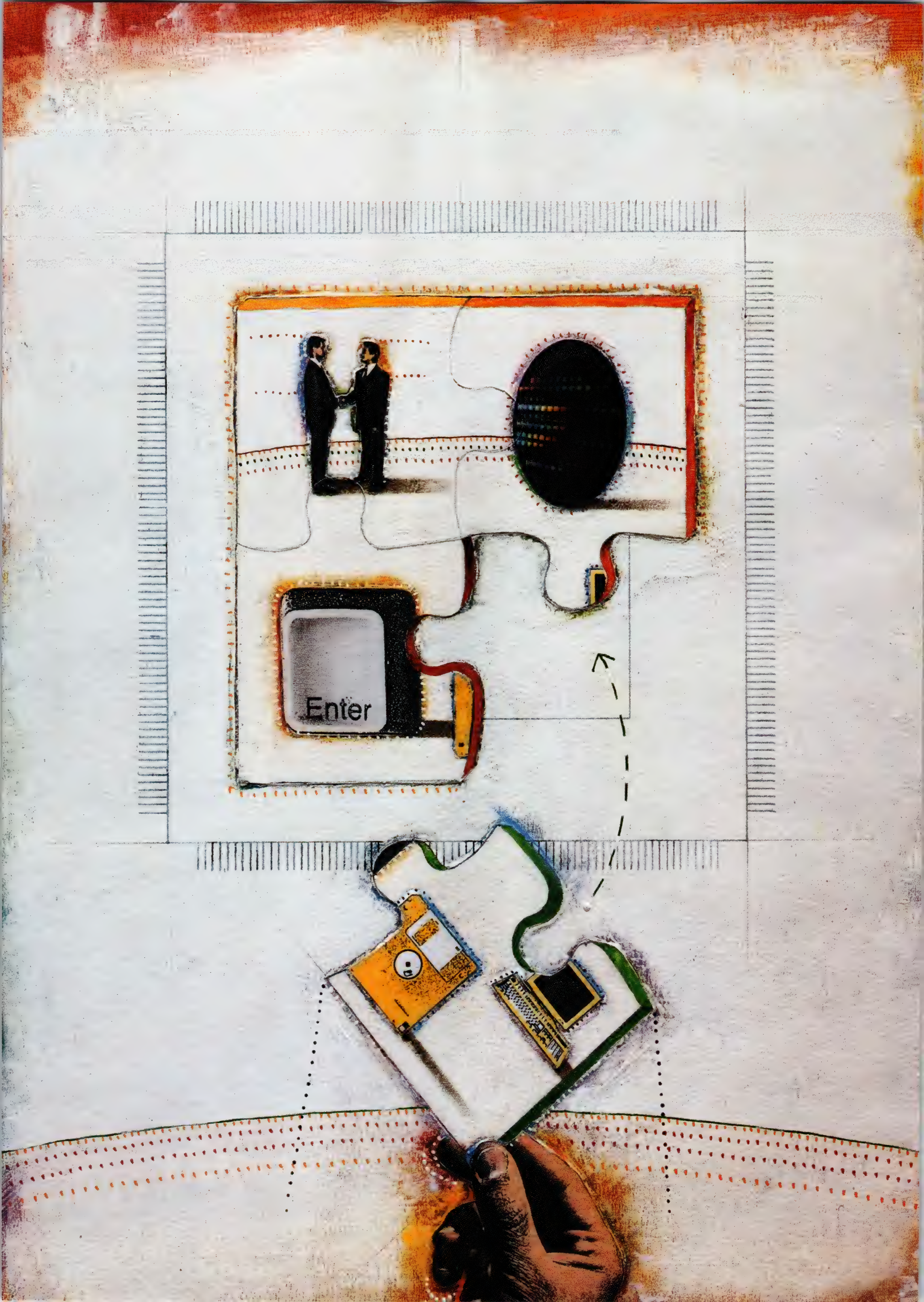
CIRCLE 215 FOR U.S. RESPONSE CIRCLE 216 FOR RESPONSE OUTSIDE THE U.S.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TI announces Total Integration.™ Integration beyond silicon.

It's a changing world. No longer is it a matter of how many circuits you can squeeze onto a chip. Today the challenge is the integration of entire systems.

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Today the guiding principle behind our semiconductor business is the concept of Total Integration.™ It is our complete focus to help you reach your next level of integration faster than ever before, with products that are better than ever before.

Extend your reach without extending your risk. In the electronics industry, the greatest rewards often have the greatest risks associated with them. At Texas Instruments, our approach to Total Integration helps you manage the risks from product development through production. And you can count on our design assistance to help reduce risk. You see, we've worked with teacher-customers worldwide to better understand the problems you face when designing a product.

Silicon solutions for your next level of integration. Faster. Smaller. Cheaper. The demands are endless. That's why we've invested nearly $6 billion in the last five years in both leading-edge R&D and a state-of-the-art global manufacturing base. All this to offer you a road map to integration today for your future product generations.

Building on our broad base of standard digital, analog and mixed-signal functions, we've developed new cores like SuperSPARC™, microSPARC™, TI486SLC and DSPs. We've introduced a variety of options for creating user-specific ICs that are based on analog and digital reusability as well as simple building-block techniques.

Tools that help you build on what you've already built. Having the silicon technologies is just the first step. To actually move from concept to system, you have to have the right tools. So we've teamed with multiple hardware and software vendors to provide tools that not only can run on open, industry-standard platforms but are road-mapped and reusable. Two recent examples: TI and Mentor Graphics are developing an open, industry-integrated tool set for on-chip integration of mixed-signal and power functions. Working with Cadence Design Systems, we will install the ASIC WorkBench™ in TI design centers around the world, simplifying the design of embedded arrays.

Design information that puts your product on the map sooner. Speed your preproduction phase simply by accessing the right information at the right time. All of our product information will be able to reach your desk top via local sources of product data. And with Electronic Data Interchange, you can have instant access to our international network of design centers for exchange of design information. We also offer simulation models for virtually all of our ICs.

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CIRCLE 204

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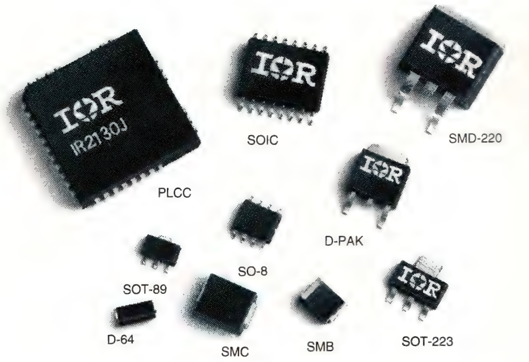

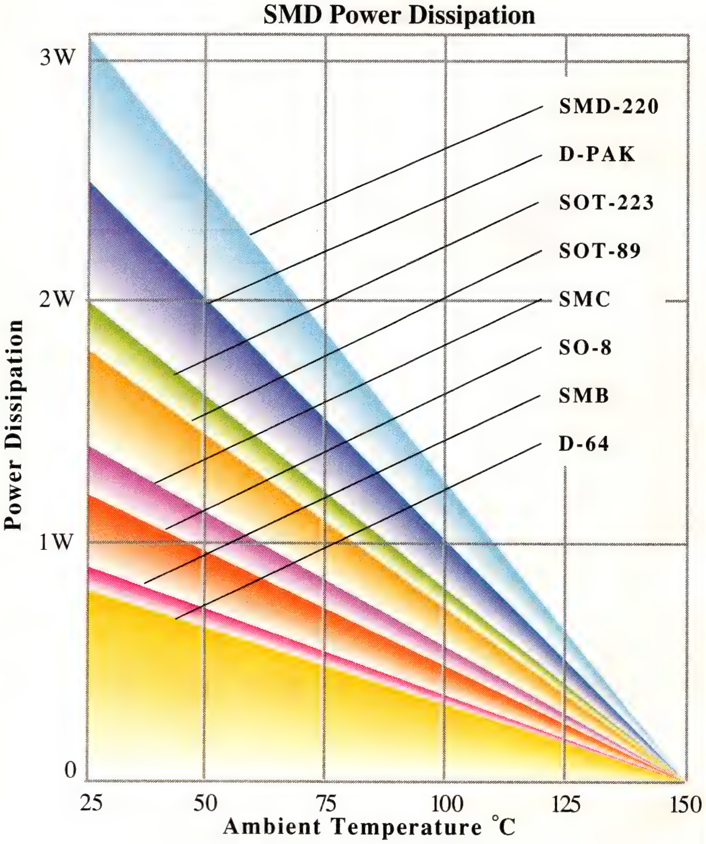

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CIRCLE 187 FOR U.S. RESPONSE   CIRCLE 188 FOR RESPONSE OUTSIDE THE U.S.

TECHNOLOGY NEWSLETTER

JOINT R&D TARGETS NEW MATERIALS, PROCESSES

A cooperative research program will focus on the development of advanced materials and more efficient and safer materials-growth processes for compound semiconductor materials. The program is the first stage of a joint R&D effort between Motorola Inc., Mesa, Ariz., and Sandia National Laboratories, Albuquerque, N.M. Some targeted applications include high-power semiconductor lasers, photonic ICs, ultra-high-speed electronics for radar and signal processing, and IR imaging sensors. One of the program's first projects will center on the development of novel high-speed, low-power-consumption aluminum-nitride and gallium-antimonide/indium-arsenide semiconductors. Sandia will provide its expertise in molecular-beam epitaxy material growth, surface physics analysis, advanced materials characterization, materials theory, and device process development. Motorola will add its expertise and resources in advanced device and circuit design and fabrication tools. A second agreement between the two companies will attempt to advance the capabilities of metal-organic vapor-phase epitaxy to create near-perfect compound semiconductors. Part of the research will also aim at developing an experimental and theoretical understanding of the chemistry of improved reactants used to manufacture the devices. Contact Peter Esherick at Sandia at (505) 844-5857. *DB*

PLUG AND PLAY BIOS SPEC IS FINALIZED

A coalition of more than 20 hardware and software companies released the Plug and Play BIOS specification that simplifies PC configuration for end users. It's now available free of charge for designers of future compatible systems. The standard was developed by Compaq Computer Corp., Houston, Texas, and Phoenix Technologies Ltd., Norwood, Mass., as part of a working group, with input from such companies as Microsoft and Intel. PCs that fall within the Plug and Play BIOS specification will seamlessly interact with the other two Plug and Play components—the operating system and I/O devices. To be compatible, the system BIOS must supply an identification and configuration of system board devices, which include the disk drives, RAM, and math coprocessor. Systems that are completely compatible will internally resolve all conflicts to guarantee bootup every time an I/O device is added or eliminated. The first PCs to employ the Plug and Play BIOS should appear early next year. For more information on the specification, contact Compaq at (713) 374-8316 or Phoenix at (714) 440-8000. *RN*

INTERCONNECT LANGUAGE SPANS DESIGN DOMAINS

The interconnect description language (IDL) defines structures in both the electrical and physical domains, helping signal-integrity tools link behavioral modeling with structural descriptions for top-down physical design of boards, multichip modules, and backplanes. IDL, developed by Cadence Design Systems Inc., San Jose, Calif., is the common thread that binds the pieces of the company's signal-integrity solution together. The geometry extractor, field solver, interconnect library, closed-form algorithms, and multiconductor simulator communicate through the interconnect language. IDL allows for both detailed Spice-level and higher-level parametrized definitions of interconnect. Early in the development cycle, engineers can use IDL to define behavioral interconnect models for pre-layout technology and space exploration. The fundamental goal of these explorations is to generate design rules that subsequently guide the physical design process. For more information about Cadence's IDL and signal-integrity environment, call the company at (408) 943-1234. *LM*

HP OPENS INSTRUMENT DRIVER SPECIFICATION

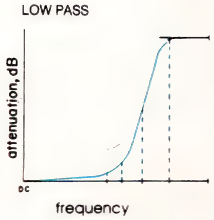
Suppliers of I/O cards now have license-free open access to Hewlett-Packard's Standard Instrument Control Library's driver-development specification. As a result, card suppliers are able to create a single Standard Instrument Control Library driver for their cards or controllers that can be leveraged across a number of applications. HP says this should make it easier for engineers and technicians writing test-and-measurement applications to interconnect their hardware. Eventually, they will be able to employ the same data-acquisition and analysis programs on various platforms without having to learn how to use different control libraries, the company says. HP announced the opening of access to the library along with release of Microsoft Windows and Windows NT software versions. It's also available with HP-UX operating systems. HP will charge a nominal fee to application developers who distribute the library with their application. *JN*

FILTERS

dc to 3GHz from $\$11^{45}$

lowpass, highpass, bandpass

- less than 1dB insertion loss
- greater than 40dB stopband rejection
- surface-mount
- BNC, Type N, SMA available
- 5-section, 30dB/octave rolloff
- VSWR less than 1.7 (typ)
- rugged hermetically-sealed pin models
- constant phase
- meets MIL-STD-202 tests
- over 100 off-the-shelf models
- immediate delivery



low pass, Plug-in, dc to 1200MHz

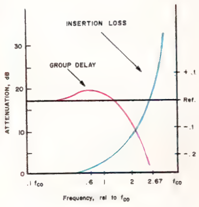
Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-5	DC-5	8-10	10-200	★LP-250	DC-225	320-400	400-1200
★LP-10.7	DC-11	19-24	24-200	★LP-300	DC-270	410-550	550-1200
★LP-21.4	DC-22	32-41	41-200	★LP-450	DC-400	580-750	750-1800
★LP-30	DC-32	47-61	61-200	★LP-550	DC-520	750-920	920-2000
★LP-50	DC-48	70-90	90-200	★LP-600	DC-680	840-1120	1120-2000
★LP-70	DC-60	90-117	117-300	★LP-750	DC-700	1000-1300	1300-2000
★P-90	DC-81	121-137	167-400	★LP-800	DC-720	1080-1400	1400-2000
★LP-100	DC-98	146-189	189-400	★LP-850	DC-760	1100-1400	1400-2000
★LP-150	DC-140	210-300	300-600	★LP-1000	DC-900	1340-1750	1750-2000
★LP-200	DC-190	290-390	390-800	★LP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

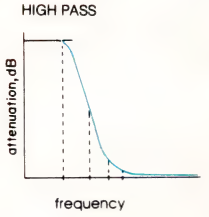
Price, (1-9 qty), all models: $11.45



Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2.67fco X̄
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

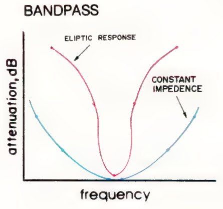
Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.



high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-25	DC-13	13-19	27.5-200	1.8:1	★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-50	DC-20	20-26	41-200	1.5:1	★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-100	DC-40	40-55	90-400	1.8:1	★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-150	DC-70	70-95	133-600	1.8:1	★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-175	DC-70	70-105	160-800	1.5:1	★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-200	DC-90	90-116	185-800	1.6:1	★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-250	DC-100	100-150	225-1200	1.3:1	★HP-1000	DC-550	550-720	1000-2200	1.9:1
★HP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95



bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

CIRCLE 105 FOR U.S. RESPONSE

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F132 1-2 REVC

SI/GE HBT PROCESS TO LEAD TO NEW RF ICS

A joint effort between two companies, each with an advanced IC process, will culminate in a broad line of ICs for analog signal and RF applications. Analog Devices, Norwood, Mass., will ultimately design and market these devices. The products will complement the company's existing line of DSP ICs, as well as voice- and base-band data converters now used in wireless applications, such as European Groupe Speciale Mobile (GSM) cellular telephones. Analog Devices will employ its own XFCB bonded-wafer complementary bipolar process, and, where necessary, IBM's silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) process. IBM along with Analog Devices developed a 1-GHz, 12-bit digital-to-analog converter (DAC) on the SiGe process, which has achieved f_ts in excess of 100 GHz and beta Early voltage products approaching 50,000. The SiGe process, as well as the 1-GHz DAC, will be described in several papers at next week's International Electron Devices Meeting (IEDM) at the Washington, DC, Hilton Hotel. For additional information, contact Doug Grant of Analog Devices at (617) 937-1481. For IEDM information, call (202) 986-1137. *FG*

FRENCH TECHNOLOGIES SEEK U.S. PARTNERS

In a flurry of meetings early last month, close to 60 different high-technology companies based in France presented their software and hardware expertise to a gathering of U.S. technology authorities and corporate executives. The companies hope to strike up various technology licensing deals and product marketing arrangements. Participating in the conference were French firms that offer scientific and engineering software, such as Chorus Systems, Communication Intelligence, Cora, Dolphin Integration, Hyperparallel Technologies, Inria, Isen, Neuro Concept, OPL France, RDC, Simulog, Straco, and Scopus Technology. Software tools for artificial-intelligence application development and imaging applications were also highlighted by Acknosoft, Advance, Ingenia, Mimetics, Pixibox, Rosenthal Chronologics, and Volumm. In addition, the area of networking and telecommunications had representatives from Dassault AT, FTP Software, Penstar Wireless, Silicon Ingenierie, Transrush, Velec, and the Wollongong Group. They described new communications hardware that included a 10-Mbit/s wireless modem as well as network-management tools. For more information, contact Patricia Pouliquen at the French Trade Commission in San Francisco, Calif., at (415) 781-0986. *DB*

COMPANIES TO PRODUCE PCMCIA SECURITY KEYS

Based on a broad technology agreement and strategic alliance between AMP Inc., Harrisburg, Pa., and Atmel Corp., San Jose, Calif., AMP will manufacture PCMCIA-compatible memory cards. Atmel will supply single-voltage flash and EPROM devices for the cards. The cards, which are available with 150- or 200-ns read-access times, fit the Type 1 (3.3-mm high) form factor. In addition to basic memory cards, the devices will be sold as electronic security keys for portable data carriers. The security keys are based on a unique Atmel device that contains a one-time 40-bit programmable identification code. The flash and EPROM cards have a capacity of 8 Mbytes, using 3- and 5-V chips. For more information, call AMP at (800) 522-6752 or Atmel at (408) 441-0311. *RN*

BEHAVIORAL SYNTHESIS YIELDS WORKING SILICON

Engineers at the Delco Electronics IC Design Center, Kokomo, Ind., claim to be the first electronics manufacturer to produce working ICs from a totally automated environment consisting of behavioral synthesis and high-level physical design tools. The ICs were developed using the AutoCircuit behavioral synthesis technology from the General Motors Research and Development Center, Warren, Mich., and high-level physical design tools developed by Cascade Design Automation, Bellevue, Wash. Much of the source code for AutoCircuit was initially written by graduate students at Carnegie-Mellon Univ., Pittsburgh, Pa. The Delco engineers created two digital-signal-processing (DSP) chips over a four-month period. The company achieved first-silicon success with both ICs using its 0.8-μm process. The engineers used the Verilog language to describe their DSP algorithms. Following simulation of the algorithms, AutoCircuit converted them into a Verilog net list of datapath modules, such as adders, subtractors, ALUs, and state machines. Then, the synthesized Verilog net lists were fed directly into Cascade's tools, which automatically compiled all of the datapath modules and synthesized the state-machine control-logic modules. The Cascade tools placed and routed the modules, and extracted post-layout timing information for gate-level timing simulation. For more information about the project, call Cascade Design Automation at (206) 643-0200, or Delco Electronics Corp. at (317) 451-0655. *LM*

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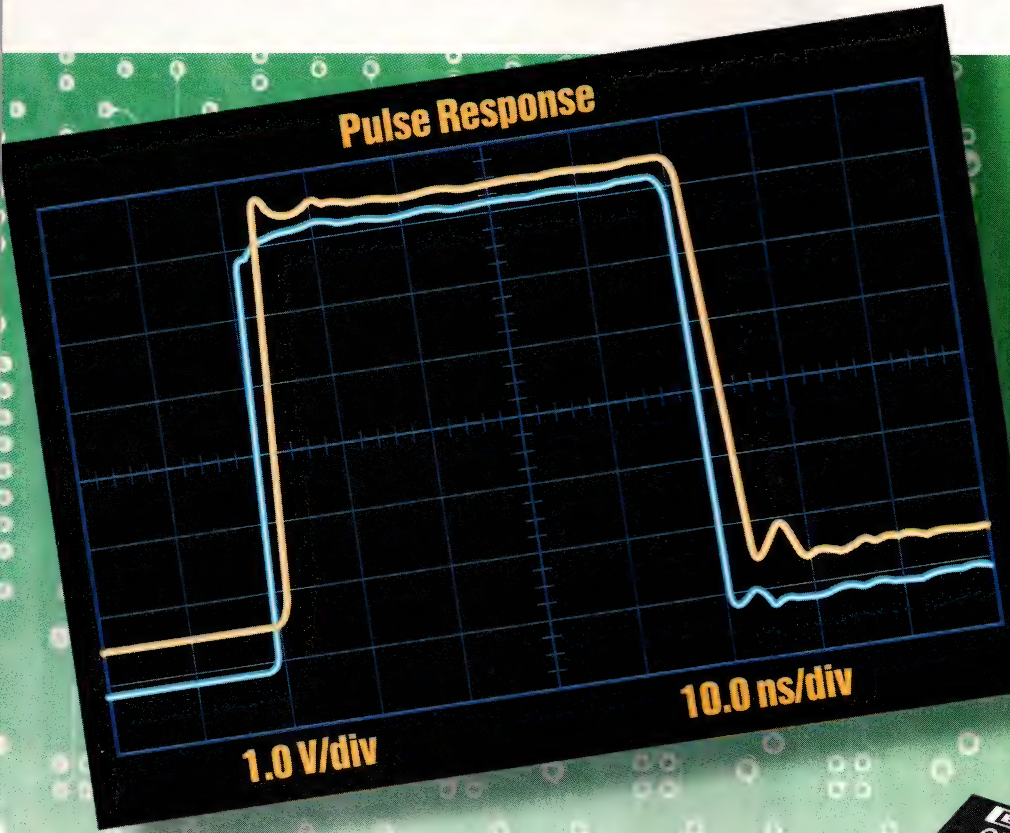
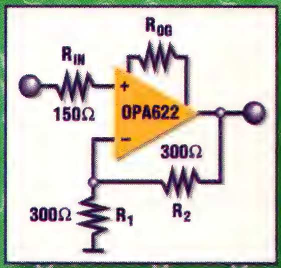
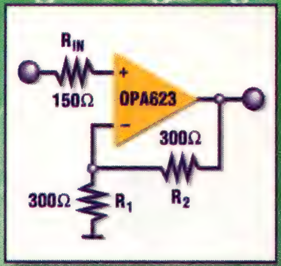
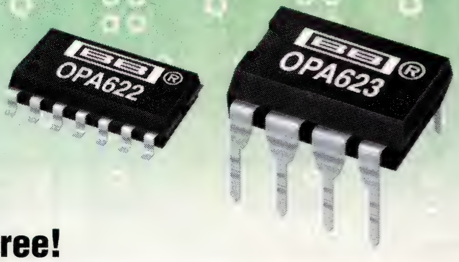
New High Speed Op Amps









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	OPA622	OPA623
Bandwidth (2.8Vp-p)	250MHz (VF)	350MHz
Slew rate	1700V/µs	2100V/µs
Rise time	2.4ns	1.9ns
Quiescent current	±5mA	±4mA
Gain flatness (DC to 30MHz)	0.12dB	0.05dB
Output current	±70mA	±70mA
Settling time, 0.1%	17ns	9ns

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PROGRESS REPORT

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Fifty years ago, getting the "big picture" at home depended mostly on your powers of imagination. But the pictures to be delivered to homes within this decade may exceed what all but the most ardent futurist *ever* imagined.

Sharp's ultra-compact DBS tuners — with their advanced designs, reduced component count and low power consumption — contribute to smaller system sizes and have established new paradigms for reliability and integration.

The TV set is the most likely point of confluence for all the innovations in information exchange now converging on the home market, with every media from video disks to fiber optic highways jostling for position. At Sharp, we've always been partial to the path of least resistance — the airwaves — ever since we created and marketed the first mass-produced crystal radio sets back in 1925.

You might be surprised at the number of areas in which Sharp continues to be the pacesetter in wireless communications components. Whether your transmission is in RF or IR bandwidths, by terrestrial or satellite broadcast, across the continent or across the room, here's why it pays to have Sharp go to bat for you.

H/V linear and R/L circular polarization LNBs from Sharp provide superior cross-polar discrimination, plus a waterproof, airtight structure which ensures reliable performance in the most severe conditions.

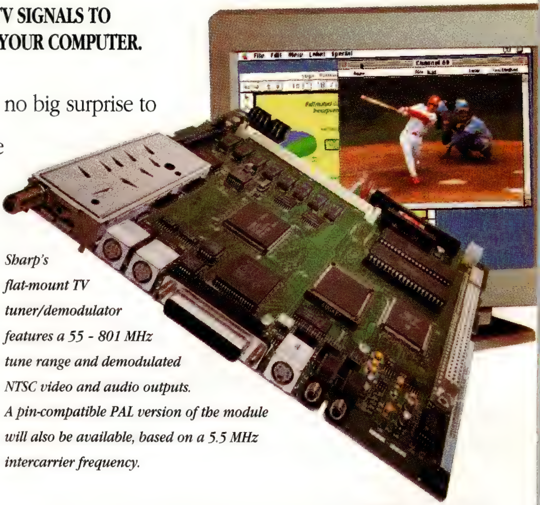
A FINE LINE OF RF COMPONENTS, FINE-TUNED TO YOUR NEEDS.

For years, Sharp has led the field in the miniaturization, noise reduction and seamless integration of RF components, from Ku band LNBs — the industry's smallest — to 22cc DBS tuners. The breadth of Sharp's line and our ability to custom-configure help us meet your size, packaging or power requirements readily.

As North American DBS comes into its own, we'll be there to bring home whole *new* generations of products supporting, for example, the transmission of multiple signals and vast home programming options — the products of *your* imagination.

From the crystal radio to the wire

WE BRING TV SIGNALS TO THE HEART OF YOUR COMPUTER.



Sharp's flat-mount TV tuner/demodulator features a 55 - 801 MHz tune range and demodulated NTSC video and audio outputs. A pin-compatible PAL version of the module will also be available, based on a 5.5 MHz intercarrier frequency.

It should come as no big surprise to see that Sharp, the world's leading manufacturer of RF components, is one of the first to deliver a TV tuner/demodulator in a flat-mount package offering easy integration in system design.

It's the start of a whole new ballgame. Manufacturers of desktop and portable PCs gain immediate entry into video and multimedia — two arenas where tuner size, mounting and power requirements precluded their entry until now. And because this is a complete component module, they can avoid design and development at the subassembly level — always an enviable competitive edge.

ess revolution: we're pulling the future out of thin air.

SHARP IS ON YOUR WAVELENGTH IN THE IR SPECTRUM, TOO.

Sharp is the first company to deliver market-ready technology for short-range high-speed infra-red data transmission. Small size, low cost, low power consumption, immunity to EMI and no FCC licensing requirements make Sharp's IR product series a key player in a nearly limitless range of new applications, from personal communications systems to wireless joysticks and interactive TV. Transmission units providing ranges up to 3 meters, higher data rates and 3-volt operation are soon to follow as Sharp continues to evolve its expertise and experience in IR communications.

Sharp's RY5 Series includes receiver, transmitter and bi-directional IR units. They support 38.4kb transmission rates over a 1-meter range, operate from a 5V source, and can be readily interfaced with existing digital circuitry.

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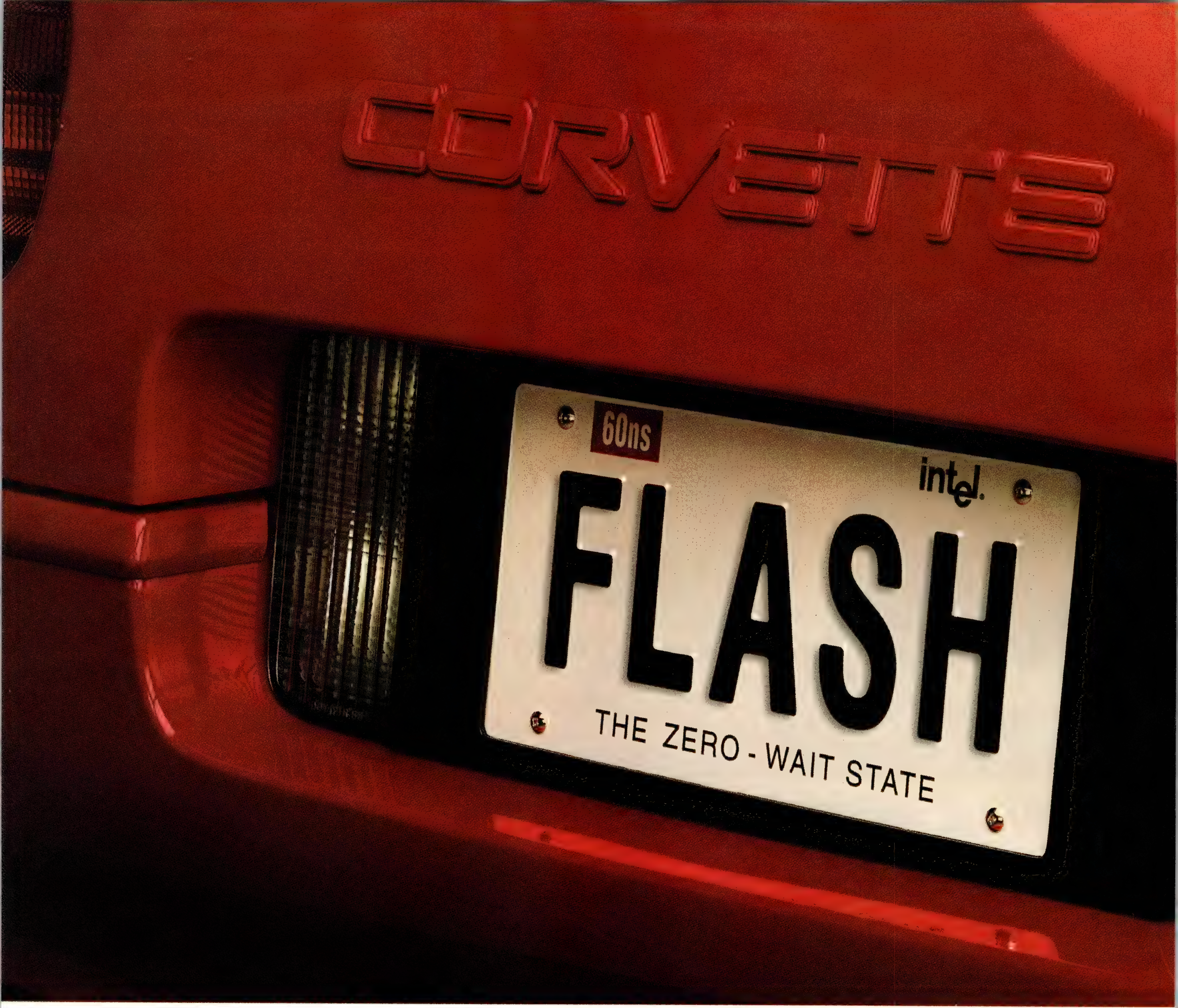
CIRCLE 128 FOR U.S. RESPONSE CIRCLE 129 FOR RESPONSE OUTSIDE THE U.S.

SEC-1093



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And with their 60ns access time, they can really bring your embedded firmware and PC BIOS designs up to speed. In fact, you'll achieve zero-wait-state performance when you use Intel Boot Block Flash with many of today's high-performance CPUs.

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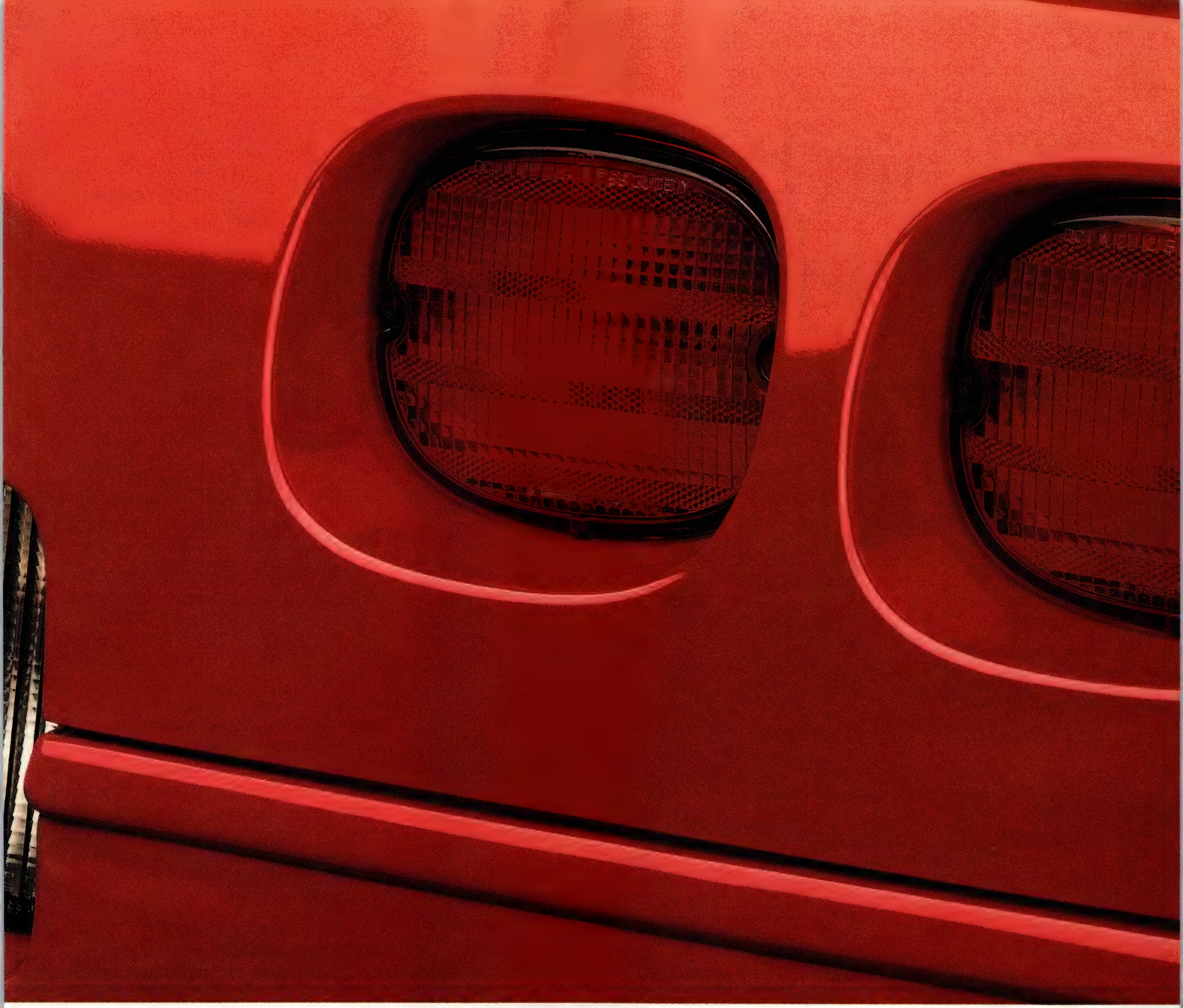

Block Flash is leading high-speed chase.

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CIRCLE 149 FOR U.S. RESPONSE

CIRCLE 150 FOR RESPONSE OUTSIDE THE U.S.

RF TRANSPONDER EMBEDDED IN AUTO IGNITION KEYS STYMIES CAR THIEVES

Despite all of the key-based security systems, lock bars, and alarm devices on the market, a skilled car thief can still break into and drive away a car in under 30 seconds. But next year in Europe, car thieves with a fondness for Fords may find their efforts thwarted by tiny RF transponders embedded in ignition keys.

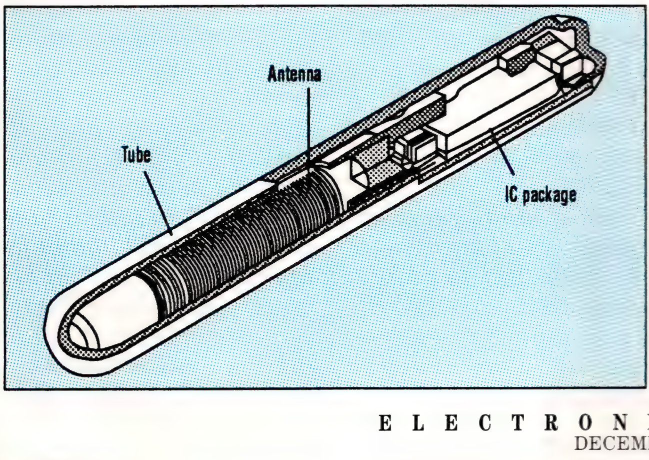
A new "vehicle immobilizing" security system, included on 1994 Ford automobiles arriving at European dealerships in October, is based on the RF Registration and Identification System (TIRIS), an identification technology developed by Texas Instruments, Attleboro, Mass. The Electronics Div. of Ford Motor Co. applied this technology to its SafeGuard anti-theft security system for use on the Escort and Fiesta models. SafeGuard may be introduced in some U.S. models by 1995.

TIRIS technology provides a tamper-proof electronic link between the driver's ignition key and the ignition system of a specific vehicle. The system uses an electronic transponder that requires no battery power to operate, but instead relies on RF pulses sent by an electronic reader located in the car's steering column *(see the figure)*.

In the Ford automotive application, the transponder probe is 22 mm long and 3.8 mm in diameter, and is located in the head of a car's ignition key. The probe contains an antenna and an EEPROM that holds a unique code specific to the vehicle, meaning that the coded key is valid for starting only that vehicle. The code, which is determined during the vehicle's manufacture, is guaranteed to be unique to within one part in 2×10^{64} codes.

The RF reader is mounted in the steering column near the ignition slot. When the ignition key is inserted and turned, the reader continuously sends out an RF pulse that's about 50 ms wide. The reader's antenna is integrated with the ignition switch and the steering-lock barrel. Its transceiver is electrically connected to the car's electronic-engine-control (EEC) module.

Upon turning the key, the transponder's antenna picks up the pulsed transmissions from the reader and stores the charge in a capacitor when the pulse is off (the off time of the pulse can be as long as needed, depending on the application). After a 1-ms delay, the transponder retrieves its unique code (in the EEPROM) and uses that code to frequency-modulate an RF signal that's sent back to the reader.



The reader next senses this returned signal, demodulates it, converts it to a serial code, and compares this code with its own code stored in the vehicle's EEC module. If the codes match, the module activates either the fuel-pump relays or the EEC itself. The entire transaction occurs in less than a second.

If, on the other hand, the reader doesn't receive the correct signal from the transponder when the ignition key is turned, the car's fuel system (or the car's electronics in some models) won't function and an alarm indication is provided. Unlike other theft-prevention systems, SafeGuard can't be overridden or hot-wired.

In some configurations of the system, a vehicle owner is provided with a master key, from which duplicate keys can be made. The master key is designed to be used for duplicating purposes only, while the slave keys are designed for the driver's key ring. Only duplicate keys made directly from the master will enable the car's engine. Should the master key be lost, the dealer or manufacturer can reproduce that vehicle's specific key.

According to TI, the system is easier to use than systems based on personal identification numbers that require users to remember and punch in a code. Also, because the transponder in the TIRIS technology is completely passive and uses no battery power, it is much more rugged than typical anti-theft systems and lasts the lifetime of the vehicle.

Conventional contact-based security systems require battery power to operate and depend on reading the contact resistance within the car's key (the key has a resistive element embedded in it). That resistance, which has to be within a certain range for the vehicle to start, can change due to normal wear and tear of the key, to the point where the car will not start. Consequently, that key must eventually be replaced.

In addition, the technology's unalterable codes offer a higher level of security according to TI. For instance, infrared systems popular in Europe can be easily overriden now that electronic stores sell low-cost equipment that can intercept and emulate an infrared signal.

The flexibility of the TIRIS RF technology will allow automotive manufacturers to adapt it to a variety of uses beyond theft prevention in the future. For example, the technology could be used to tailor the vehicle to individual needs. Separate "husband" and "wife" keys could automatically trigger seat and mirror adjustments, as well as preset preferred radio stations. A "teenager" key could limit the vehicle's top speeds. Other keys that restrict access to the trunk or glove compartment could be used when giving the car to a mechanic or valet.

Furthermore, the TIRIS technology's read range—the distance from which the transponder can be powered from the reader—of 1 m could allow for passive entry and exit applications. In these systems, the presence of the key would auto-technology has been specified for vehicle-identification applications that automate toll collection. The system will work as long as the transponder is within the vicinity of the reader to pick up the latter's RF transmissions. And the transponder can be packaged in a variety of shapes and sizes to suit the application.

For more information, contact Tony Sabetti of TI at (508) 699-1982.

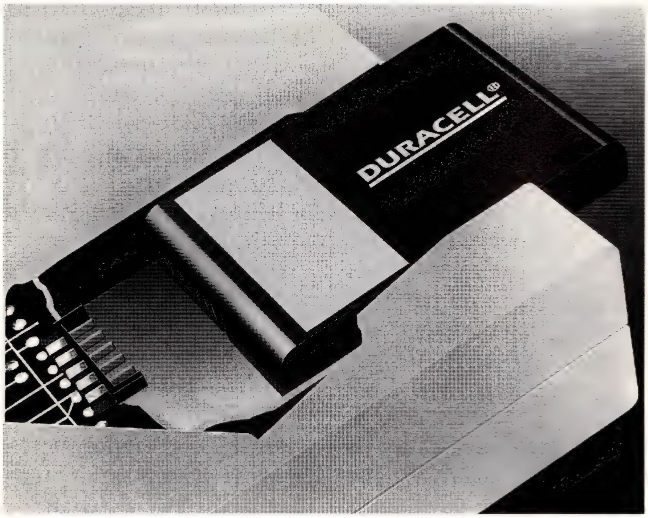
MILT LEONARD

NIMH BATTERY-PACK INTERCONNECT ADVANCES STANDARDIZATION

One year after announcing its planned line of standardized nickel-metal-hydride (NiMH) rechargeable batteries for the communication, computing, and camcorder markets, Duracell Inc., Bethel, Conn., has enlisted the aid of a major interconnection manufacturer to develop a standard battery interconnection (ELECTRONIC DESIGN, Nov. 22, p. 18). Two of four newly introduced packs for portable computers incorporate the connector scheme conceived by AMP Inc., Harrisburg, Pa.

The interconnection addresses a number of design issues while holding out the potential for shorter design cycles. According to David Griesemer, AMP's manager of development engineering, most of today's computer battery packs incorporate flat-plate-style interconnections. A number of problems are associated with these flat plates, though. For one, there's a limited amount of wiping and cleaning action as the battery pack's contacts mate with those of the computer. For another, such contacts are only slightly recessed, providing a minimal amount of protection against electrical shorting and mechanical damage. Not only that, such interconnections are typically designed on a custom basis for each battery pack, which itself is usually a custom design.

AMP's Advanced Battery-Pack Interconnect addresses these issues while extending additional advantages (see the photo). As the battery pack's recessed contacts mate with the pc-board header, a firm wiping action removes oxides that can ultimately cause discontinuity. In addition, its recessed contacts eliminate accidental shorting. Design flexibility stems from the connector's multidirectional interface that mates in more than one angle and position to give designers added versatility. Even more flexibility is attained because the battery pack and header can mate at varying heights. Polarization features prevent accidental mismating.



The interconnect is designed to automatically exert an optimum normal force on the batteries' contacts, eliminating the need for OEMs to devise external mechanisms that would force contact between batteries and contact points. The inner contact surface is nickel plating over a copper alloy. The connector is rated at 1000 mate/demate cycles for the pack side and 5000 for the header. The 1000 cycles roughly corresponds to the expected lifespan for the batteries themselves.

Other specifications for the interconnection include a current-carrying capacity of 7 A at a temperature rise of 30°C. Its operating temperature ranges from –30 to 70°C.

The four battery-pack models offer capacities of 12, 18 (in two mechanical configurations), and 27 Wh. These capacities were arrived at after extensive consultations with OEMs, as were the batteries' physical form factors. Two more packs for cellular telephones and personal digital assistants are forthcoming.

Duracell is planning ahead for standardized protocols involving communication between the battery pack and the system it powers. The packs are ready to accept an ASIC to be designed in later for intelligence features such as on-line status indication. Questions remain, however, as to how much active circuitry can be designed into the packs. One scheme may involve a partitioning of charging circuitry, in which some elements are placed inside the packs. Another avenue may be to develop a universal charger that will accept all standard packs, doing away with separate wall chargers for a telephone, computer, and camcorder.

Standardization of NiMH battery packs is intended to combat the rapid proliferation of the packs and, at the same time, establish a NiMH market for consumer electronics that's more akin to the existing non-rechargeable (alkaline) market. According to Norm Allen, Duracell's vice president of new-product sales and marketing, a small number of standard form factors makes matters easier for OEMs, retailers, and consumers alike. Duracell has formed a technology alliance with Toshiba Battery Co. Ltd., Tokyo, and Varta Batterie AG, Hannover, Germany, in its efforts to es-

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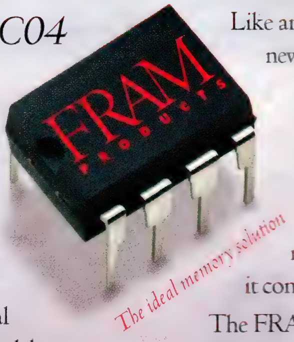

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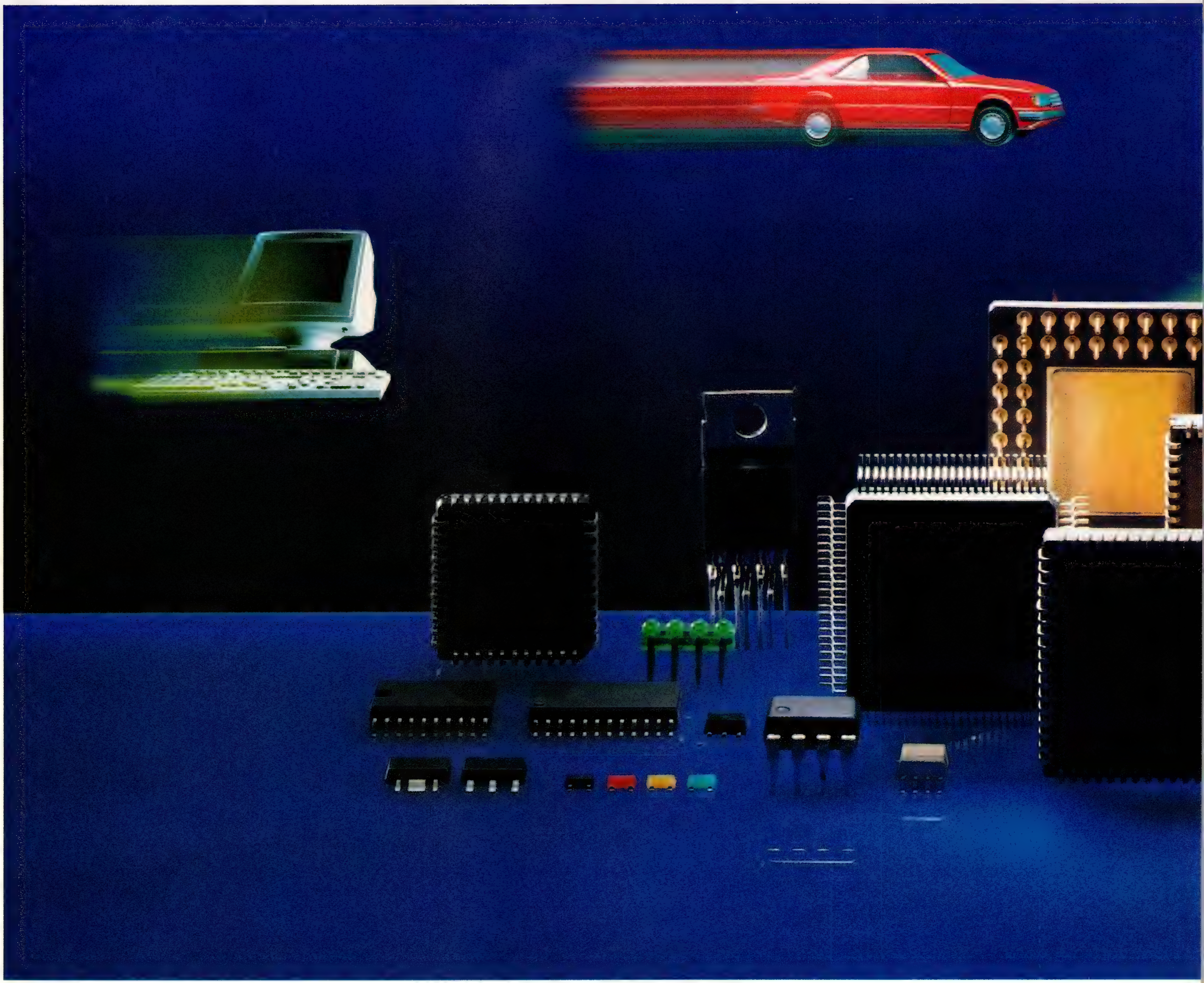
CIRCLE 126 FOR U.S. RESPONSE **CIRCLE 127 FOR RESPONSE OUTSIDE THE U.S.**

SIEMENS



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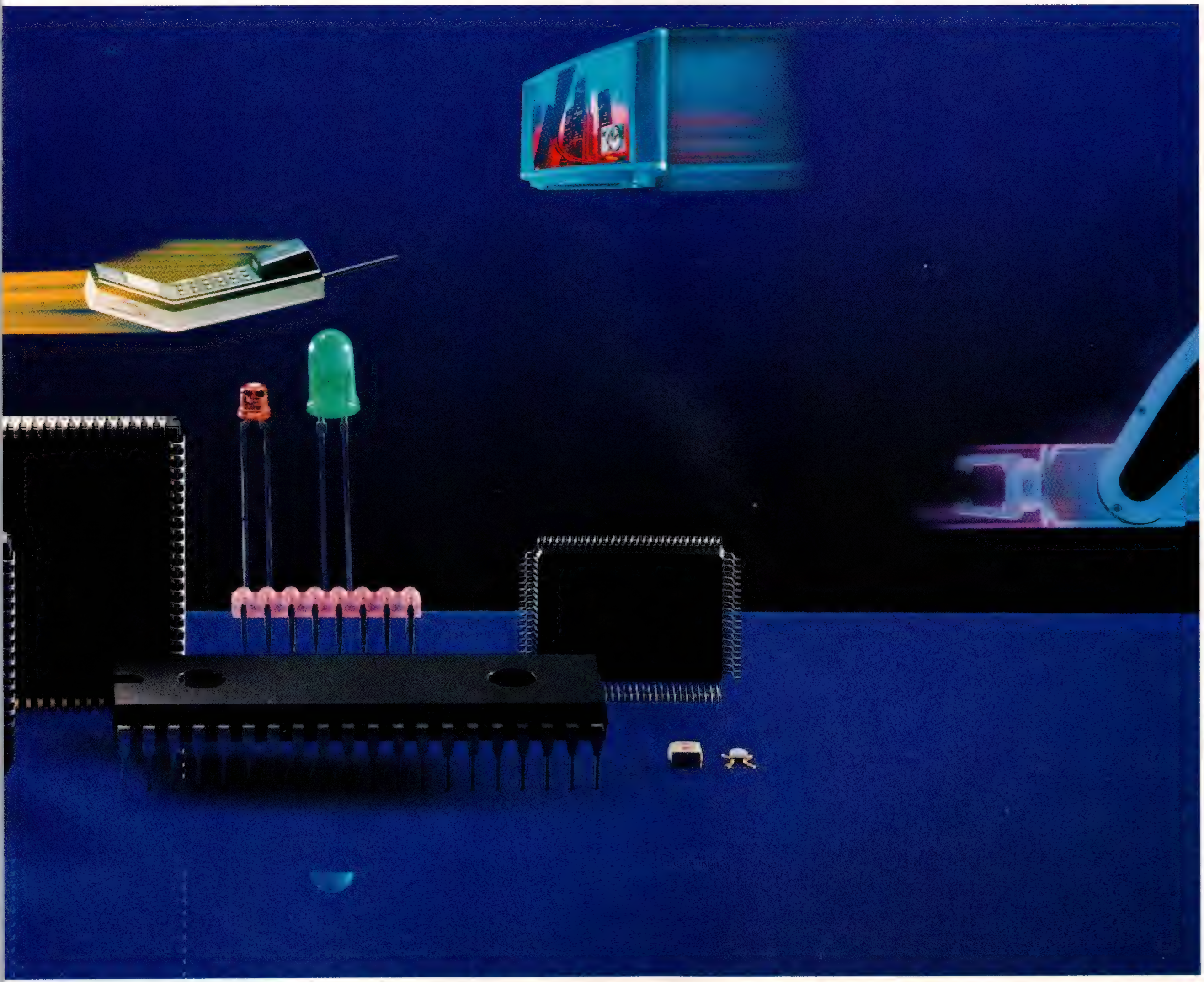

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CIRCLE 132 FOR U.S. RESPONSE

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tablish standards.

Besides the previously announced intention of Fujitsu Network Transmission Systems Inc., Dallas, Texas, to use Duracell's NiMH packs in its next generation of cellular telephones, Duracell gained at least one other major design win: According to Allen, Compaq Computer Corp., Houston, Texas, will use the packs in its next generation of notebook computers.

DAVID MALINIAK

MICROMACHINED MICROBOLOMETERS MAY LEAD TO LOW-COST INFRARED NIGHT-VISION SYSTEMS

Typical infrared (IR) night-vision imaging systems require cryogenic cooling, complex scanning optics, and high-ticket sensors. As a result, such systems can generally go for $50,000 or more, which puts them beyond the reach of most non-military applications. But a development by the Honeywell Technology Center, Bloomington, Minn., is about to change all that.

R.A. Wood, a scientist at Honeywell, reports that the company developed a low-cost IR focal-plane (staring) array that may allow night-vision camera costs to drop to less than $1000. The array is based on microbolometers fabricated on a micromachined silicon chip (bolometers are resistors whose resistance is a function of the radiated energy impinging on them). Because the device consists of an array of 240 by 336 individual pixel sensors, optical scanning isn't needed. In addition, the array operates at room temperature, and is packaged in such a way that it can be readily inserted into a camera (Fig. 1).

Each silicon microbolometer sensor consists of a 0.5-mm-thick micromachined silicon-nitride plate

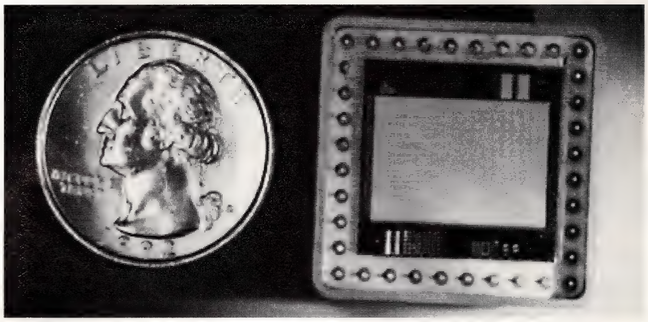

Fig. 1

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suspended clear of the underlying silicon by two legs. Silicon microbolometers are particularly suitable for room-temperature operation because their performance varies little with ambient temperature. Moreover, they can be designed at the peak of the Planck curve for room-temperature targets (8- to 12-mm wavelengths) where the atmosphere is also highly transmissive.

Readout circuits integrated into the silicon sequentially sense each of the array's 80,640 bolometers once every 33 ms. These circuits are made up of a high-speed transistor switch under each pixel and peripheral multiplexing and control circuits. External electronics located in the camera convert the bolometer signals to a TV image. The external circuits consist of a preamplifier, an analog-to-digital converter, and a single-board digital-image processor.

Mounted in a camera that's equipped with an F/1.0 lens, the imaging system has a measured thermal sensitivity of less than 0.04°C at TV frame rates. The system can produce images superior in quality compared with costlier cryogenically cooled IR systems (Fig. 2).

Dr. Wood will describe his invention at the International Electron Devices Meeting (IEDM), to be held at the Washington D.C. Hilton Hotel from Dec. 4-8. For additional information, contact Dr. Wood at (612) 956-4504. Conference information is available by calling

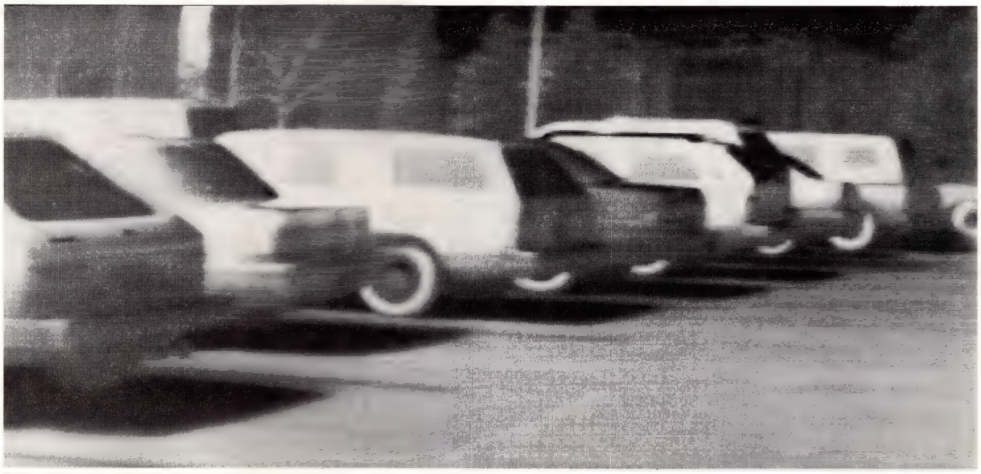

Fig.2

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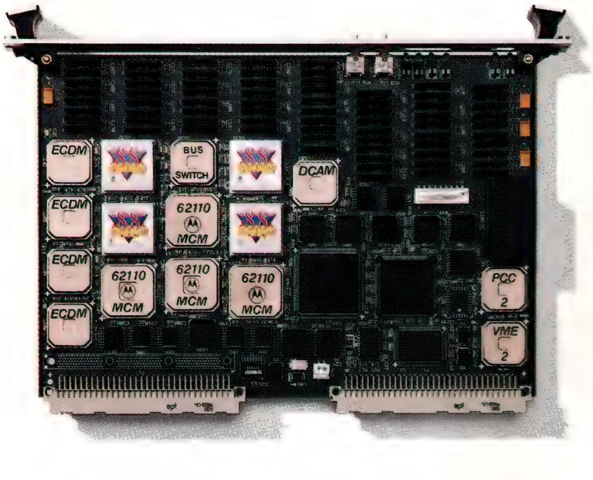
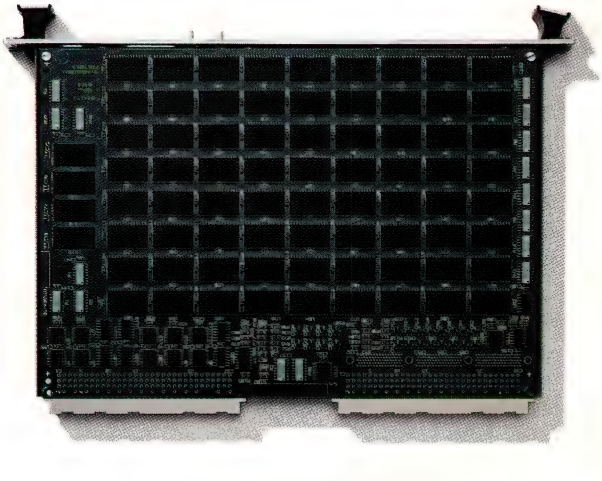


Front Side



Back Side

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ADVANCES IN DEVICE STRUCTURES AND PROCESS TECHNIQUES HERALD GIGA-ELEMENT CIRCUITS.

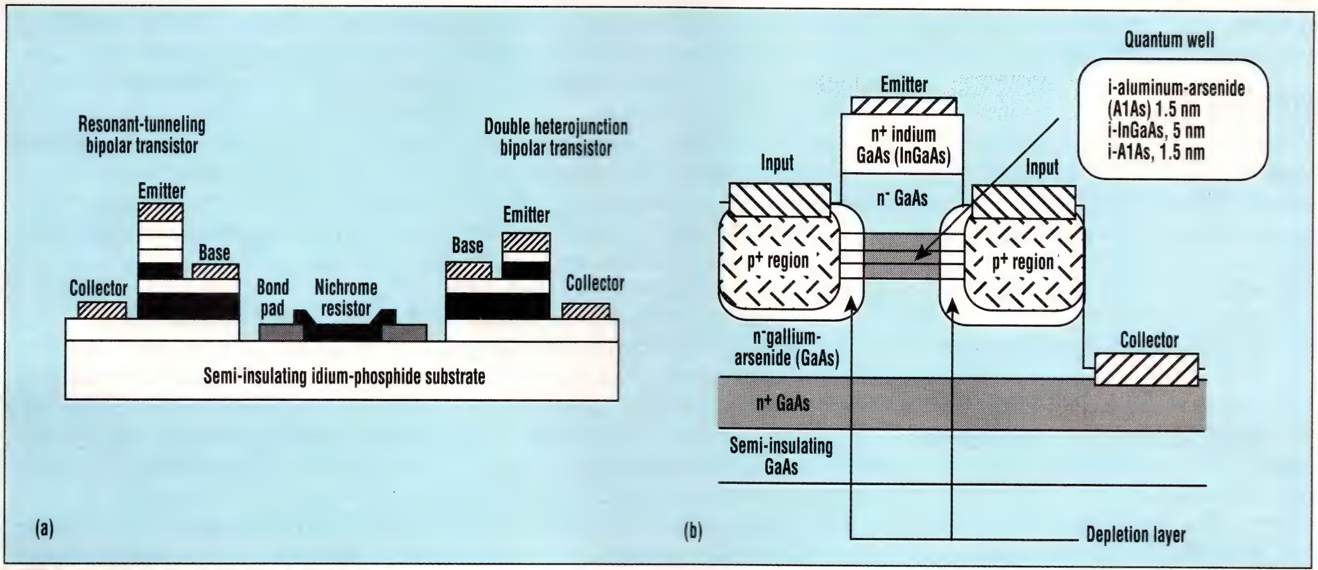
DAVE BURSKY AND FRANK GOODENOUGH

Novel device structures, finer-line processes, and new techniques for making digital, analog, and mixed-signal ICs and discrete devices are some of the topics to be described at next week's International Electron Devices Meeting (IEDM). The conference, which will be held at the Washington Hilton Hotel, Dec. 5-8, has 24 technical sessions scheduled. They will explore the latest developments in high-density logic, novel transistors, large memories, monolithic and discrete power ICs and devices, displays, sensors, detectors and imagers. Three sessions are devoted to developments in vacuum tubes, non-extinct "dinosaurs" that continue to find their way into leading-edge applications.

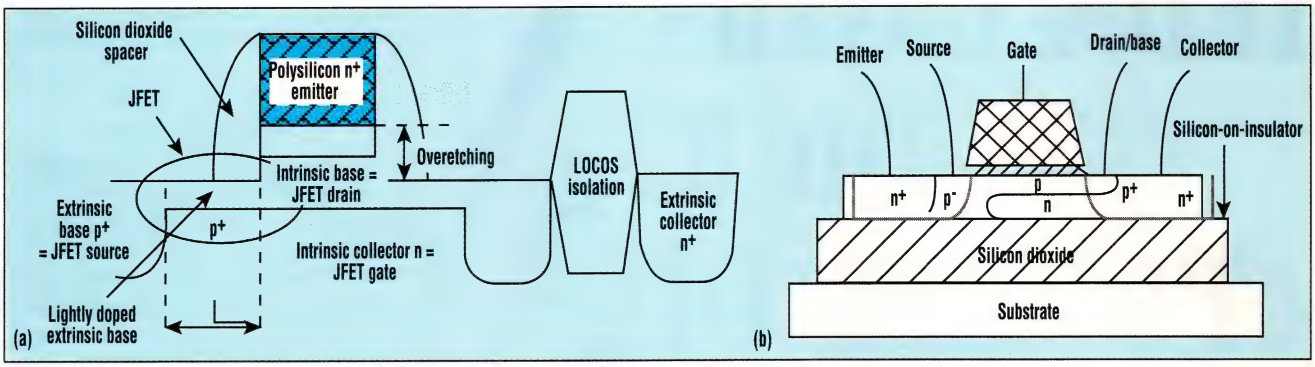
Advanced CMOS processes with gate dimensions of just 0.1 µm will also be unveiled in several conference papers. Such processes promise giga-gate density circuits. In addition, new memory cells for DRAMs and SRAMs debuting at the conference show the potential for 256-Mbit DRAMs and 64-Mbit SRAMs.

One interesting development is that of room-temperature and integrated resonant-tunneling transistors (RTTs), devices noted for their ability to combine multiple logic functions into one simple circuit. Previously, RTTs could only operate at liquid-nitrogen temperatures and were available only in hybrid form. This "hot" topic will be covered in Sessions 16 and 21.

Because RTTs can exhibit multiple on and off states that are defined as functions of the input voltage, RTT-based circuits can implement complex functions with fewer gates than conventional logic. By co-integrating resonant tunneling structures with heterojunction bipolar transistors, researchers at Texas Instruments Inc., Dallas, came up with the industry's first RTT heterojunction bipolar transistor ICs that



1. ROOM-TEMPERATURE operation of resonant-tunneling bipolar transistors fabricated on an indium-phosphide substrate was demonstrated by Texas Instruments (a). Fabricated with layers of aluminum arsenide/indium gallium arsenide/indium arsenide, both single- and dual-heterojunction bipolar transistors will implement highly efficient logic. Novel monostable-bistable transition logic elements (MOBILEs) developed by NTT combine a resonant-tunneling diode with multiple p^+/n^- junctions to efficiently implement logic functions (b).



2. TWO DIFFERENT approaches developed by CNET are used to create negative-resistance devices. The first approach employs a biCMOS structure formed with the vertical bipolar transistor and an intrinsic JFET to achieve a change of several orders of magnitude (on/off ratio) in the current flow (a). The co-integration of a lateral bipolar transistor and an accumulation-mode MOSFET in the silicon-on-insulator material keeps the device area to about the size of the MOSFET (b). Moreover, it achieves a very strong n-type negative resistance.

can operate at room temperatures *(Fig. 1a)*. The circuits, described in session 16, were implemented in a III-V heteroepitaxial process on indium-phosphide (InP) substrates, and include XOR, XNOR, Carry, and full-adder functions.

The transistor structures are fabricated with layers of aluminum arsenide/indium gallium arsenide/indium arsenide (AlAs/InGaAs/InAs) on a semi-insulating InP substrate. The researchers created both single- as well as double-heterojunction bipolar transistors on the same substrate. The transistors have an 11-GHz current-gain cutoff frequency. Maximum oscillation frequency for the single-heterojunction version is 21 GHz; the double-heterojunction devices are 59 and 43 GHz.

MOBILEs

In the same session, researchers from Nippon Telegraph and Telephone Public Corp.'s LSI laboratories, Atsugi, Japan, created a new logic gate with RTTs. Referred to as monostable-bistable transition logic elements (MOBILEs), the structures also provide high logic efficiencies and high current-drive capability that permits large circuit fan-outs. The MOBILE structure employs the monostable-to-bistable transition of a circuit, which consists of two RTTs connected serially, and drives the circuit by oscillating the bias voltage to produce the transition.

The device structure starts with a resonant-tunneling diode and multiple p^+/n^- junction gates *(Fig. 1b)*. The junction gates control the diode area and, consequently, the current let through by the diode. The number of junction gates can be increased by placing them around the emitter region (one end of the diode structure). The MOBILE performs a threshold logic function by taking a weighted sum of the input signals, because the total RTT current change is proportional to that sum and the weight is proportional to gate width.

The variable-function logic gate implemented by MOBILEs can perform 14 of the 16 possible Boolean functions for two inputs simply by choosing the correct control voltages. In one design example, researchers created a cellular automata that generates random sequences. The automata cell requires just three gates—about one-fifth the number of gates that would be required for a CMOS automata function.

Using 0.1-µm design rules, Schottky-collector AlAs/GaAs resonant-tunneling diodes were developed jointly by the University of California at Santa Barbara, and the Jet Propulsion Laboratory and the California Institute of Technology, both in Pasadena, Calif. The diodes have a maximum frequency of 850 GHz—the highest reported for AlAs/GaAs structures. The frequency was achieved by reducing the parasitic series resistance with the Schottky contact rather than the typical n^+ collector and ohmic contact.

Negative-resistance devices hold great potential for application in analog circuits, as well as in high-density SRAMs. However, most of the previously reported RTTs couldn't be integrated in silicon. That's starting to change, though, as some of the just-described papers illustrate. Researchers at CNET, Meylan, France, have also been looking at silicon-compatible negative-resistance elements. One's an offshoot of the vertical bipolar transistor often used in biCMOS processes. Another stems from a silicon-on-insulator (SOI) film that co-integrates two devices—a lateral bipolar transistor and an accumulation-mode MOSFET merged within a structure that's about the size of a MOS transistor.

In the biCMOS-based structure, thickness and length of the intrinsic JFET's channel can be optimized to increase the efficiency of the channel pinch-off effect, thereby achieving several orders of magnitude change in the current drop through the transistor *(Fig. 2a)*. The co-integration in the SOI layer lets the dual-device structure attain a very strong n-type negative-resistance characteristic when both devices are simultaneously activated *(Fig. 2b)*.

A FORWARD GLIMPSE

Even as new device structures are explored, improvements in existing structures, such as in CMOS circuits, are giving designers a view of the technology's extensibility. In an invited presentation in session 6, IBM Corp., Essex Junction, Vt., will provide a glimpse of ultra-large-scale integration as minimum lithographic features go below 100 nm and circuit complexities extend beyond 10 to 20 million gates.

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CMOS room-temperature performance will peak as minimum circuit dimensions approach 100 nm. After that, the constant power constraint reverses the trend of greater performance with increasing density. An optimal supply voltage of about 0.8 V will be used to power the circuits, which are expected to deliver about 2.5 times the performance of 0.5-μm CMOS. Going beyond the 20-Mgate level per chip will force the supply voltage down to near 0.5 V, but gate delays might actually increase. As a result, any further system performance increases must be achieved through functional integration coupled with architectural as well as circuit innovations.

Fully depleted SOI CMOS may enhance performance still further, as will the use of low temperatures. That will shift the performance barrier to a significantly smaller minimum feature size of 20 nm. Such circuits could yield performance levels 20-times those of 0.5-μm CMOS. Other innovations include using devices with multiple threshold-voltage levels to circumvent the subthreshold-leakage constraint, which permits the threshold voltage to scale with the supply voltage.

When trying to form ultra-small gates, there's also the challenge of forming extremely shallow source and drain regions. Experimenting with phosphorus source and drain junctions just 10-nm deep, designers at Toshiba Corp., Kawasaki, Japan, managed to diffuse the phosphorus from a phosphorus-silicate glass (PSG) film. Described in session 6, the shallow diffusion complements the 40-nm-wide (0.04-μm) gates fabricated, yet normal MOSFET operation at room temperature was still achieved. The researchers think these are the smallest room-temperature MOSFETs to date.

Another presentation by IBM in the same session will describe 0.1-μm gate MOSFETs operating with a 1.5-V supply. The transistors employ dual n^+/p^+ polysilicon gates and 35-Å gate oxides. Resulting circuits yielded delays of just 22 ps/stage on an inverter-type ring oscillator, the fastest switching speed reported. Delays drop to 17 ps if the circuit's supply level is raised to 2.5 V. To form such small-dimension devices, five electron-beam lithographic steps and eight optical mask levels were used.

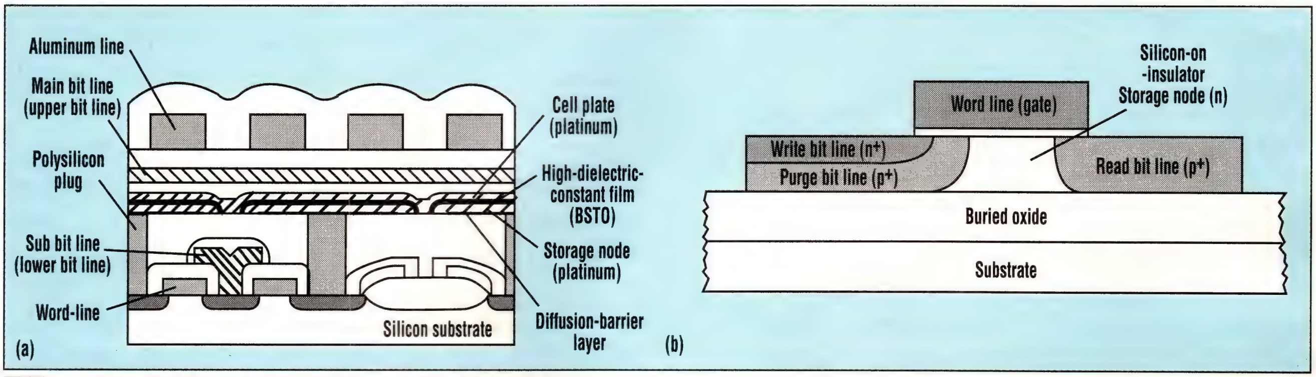
Researchers at AT&T Bell Laboratories, Holmdel, N.J. are also working on 0.1-μm devices, described in session 6 as well. Their creation delivers ring-oscillator stage delays of 11.8 ps when the circuits are powered by a 2.5-V supply—yet another record-setting level for room-temperature operation on bulk-silicon substrates. To form the transistors, AT&T's designers employ vertical-doping-engineered structures to provide high cutoff frequencies and good subthreshold and drain characteristics.

The structures also use high-energy well implants to form retrograde well profiles to reduce junction capacitance. To control drain-induced barrier lowering, the designers added a lateral local doping structure in the channel region by using a shallow implant. A deep implant is used to control bulk punch-through without increasing source-drain junction capacitance.

NEW SMALL GATE SCHEMES

New gate structures and process schemes for small-dimension gates, ranging from 0.15 to 0.25 μm, are examined in sessions 34 and 36. One such example involves devices made on a 0.15-μm CMOS process developed by NEC Corp., Tokyo, Japan. Optimized for operation from a 1.9-V supply, the structures delivered switching speeds of about 27 ps. In NEC's structures, a 5-nm gate oxide was employed along with shallow source/drain extensions, titanium-salicided ($TiSi_2$) source/drain contacts, and area-restricted channel implants.

Use of trench isolation demarcates a 0.2-μm CMOS process developed by NTT's LSI Laboratories, Atsugi, Japan. With the isolation afforded by the shallow trenches, NTT fabricated clocked-inverter 1/16 frequency dividers that operate from 1.41 to 6.08 GHz when powered by a 2-V supply. Larger-dimension circuits, fabricated with 0.3-μm n-channel and 0.6-μm p-channel MOSFETs, operated at 273 MHz with a 1-V supply and consumed just 3.25 μW. At 1.41 GHz and with a 2-V supply, power consumption is just 63.2 μW—the lowest power-frequency ratios reported to date.



3. A STACKED-CAPACITOR DRAM CELL, developed by Mitsubishi, employs a high-dielectric-constant film to provide a capacitance of more than 25 fF in an area just 0.72 μm^2. The film consists of barium-strontium and titanium-oxide, and is sandwiched between two platinum plates (a). A capacitor-less DRAM cell, fabricated in the isolated silicon layer of a silicon-on-insulator substrate, was created by the University of California at Berkeley (b). The capacitor is actually formed in the silicon "body" region. To control the reads and writes, a single transistor site includes an n-channel Write MOSFET and a p-channel Read MOSFET.

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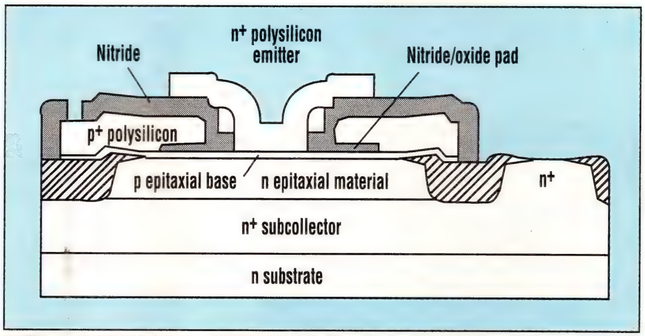

4. THIS NON-SELF-ALIGNED silicon-germanium heterojunction bipolar transistor, developed by IBM, achieves an f_t of 113 GHz and a βV_A product of 48,400 V.

Memory circuits are prime beneficiaries of the improved processes and finer-line lithography. In session 26, several papers examine trench and stacked-cell structures that may find their way into future 256-Mbit and 1-Gbit DRAMs. These cells, some based on trenches, are based on 0.25-μm lithographic ground rules and will occupy areas as small as 0.605 μm^2. Such a cell, described by the joint research team of IBM Corp., Hopewell Junction, N.Y.; Siemens AG, Munich, Germany; and Toshiba Corp. is about 25% smaller than a conventional trench cell. It employs a self-aligned buried strap.

The strap (a trench-to-device connection) is defined by the intersection of the deep trench storage node and the shallow trench isolation. The isolation helps keep the array leakage to less than 0.1 fA/cell with a supply voltage of 2.5 V. That low leakage value would allow charge retention times of several seconds.

Going above the substrate, a simple stacked-capacitor cell developed by Mitsubishi Electric Corp.'s ULSI laboratories (located in Hyogo, Japan) employs a high-dielectric-constant film to provide a capacitance of more than 25 fF in a cell size of just 0.72 μm^2 *(Fig. 3a)*. The capacitor features a planar structure with an equivalent silicon-dioxide (SiO_2) thickness of 0.5 nm, achieved by using a barium-strontium titanium-oxide (BSTO) film, platinum cell plates, and storage node contacts. Mitsubishi expects such a cell to be usable in 256-Mbit-generation DRAMs.

In another paper, Toshiba will disclose some of the cell details of its NAND-based DRAM described at this past February's International Solid State Circuits Conference. According to Toshiba, the NAND-type cell topology could serve for both 256-Mbit and 1-Gbit generations of DRAMs. That's because it simplifies the interconnection structures on the chip, permitting a more compact circuit layout.

Any space occupied by the storage element, though, replicated 256 million or more times, will consume a considerable amount of chip area. A novel scheme, to be described in session 26 by researchers at the University of California at Berkeley, eliminates the capacitor storage element by implementing the DRAM on an SOI substrate. The capacitor-less DRAM, which possesses a large read current, uses the floating body of the SOI region below the gate for charge storage *(Fig. 3b)*.

A write n-channel MOSFET and a read p-channel MOSFET are integrated into the dimensions of a single transistor, further saving chip area. The cell operation includes Purge/Write and Read cycles that use a combination of four voltage levels to control memory operation. Capacitor-less cells can be laid out in two-dimensional contactless arrays, resulting in the achievement of very high memory densities.

SOI technology also plays an important role in future-generation SRAMs, which all seem to be moving to 3D storage cells with p-channel thin-film transistor (TFT) loads above the substrate. For instance, a novel toroidal TFT structure will be unveiled by Motorola Inc., Austin, Texas, in session 33. The structure was fabricated using a modified biCMOS process with which the company is currently tuning for 16-Mbit SRAMs. The toroidal-shaped TFTs have an on-off ratio of 2×10^4 at 2.5 V and greater than 10^5 at 3.3 V.

A symmetrical memory cell optimized for 64-Mbit SRAMs will be detailed in the same session by researchers from Sony Corp.'s ULSI laboratories, Kanagawa, Japan. The TFT-based cell has on-off ratios as high at 10^7 at 2.5 V. Such high on-off ratios translate into low leakage currents—just 2.5 fA/cell—resulting in a standby current of just 200 nA in a 64-Mbit SRAM. The symmetrical cell starts at the bottom gate of the TFT, which is formed with the second and third polysilicon layers, while the fourth and fifth polysilicon layers are ground plates that form a capacitor to improve soft-error immunity. Yet additional SRAM cell ideas will be presented by Hitachi Ltd., Tokyo, and IBM Corp., Yorktown Heights, N.Y.

SiGe Goes Analog

Improvements in analog processes also stand out at the IEDM, evident by a pair of presentations in session 4 by teams from IBM's Research Division in Yorktown Heights. They developed a silicon-germanium (SiGe) 2-V heterojunction-bipolar-transistor (HBT) process sporting devices that combine f_ts reaching over 100 GHz with a beta-Early-voltage product (βV_A) of over 48,000—a product usually associated with 20-year-old, 40-V, 600-MHz standard bipolar processes. It turns out that adding the germanium not only raises the f_t, but raises the βV_A as well.

In the first presentation, a team fabricated five different SiGe-transistor structures and two different silicon-transistor structures. Team members included researchers from IBM; Analog Devices, Wilmington Mass.; and Auburn University in Alabama. The process they used and its derivatives will eventually launch a new generation of silicon analog as well as RF ICs.

Whereas their optimum SiGe device had an f_t of 46 GHz, a βV_A of 6160 V, and a BV_{CEO} of 3.5 V, similar values for the optimum silicon-only device ran 31 GHz, 1176 V, and 4 V. A 12-bit, 1-GHz digital-to-analog converter (DAC) requiring only 1 W was designed and fabricated on this process with SiGe HBTs.

In the second presentation, team members describe how they optimized SiGe and silicon HBTs, but in this case they vary the amount of

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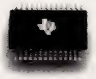

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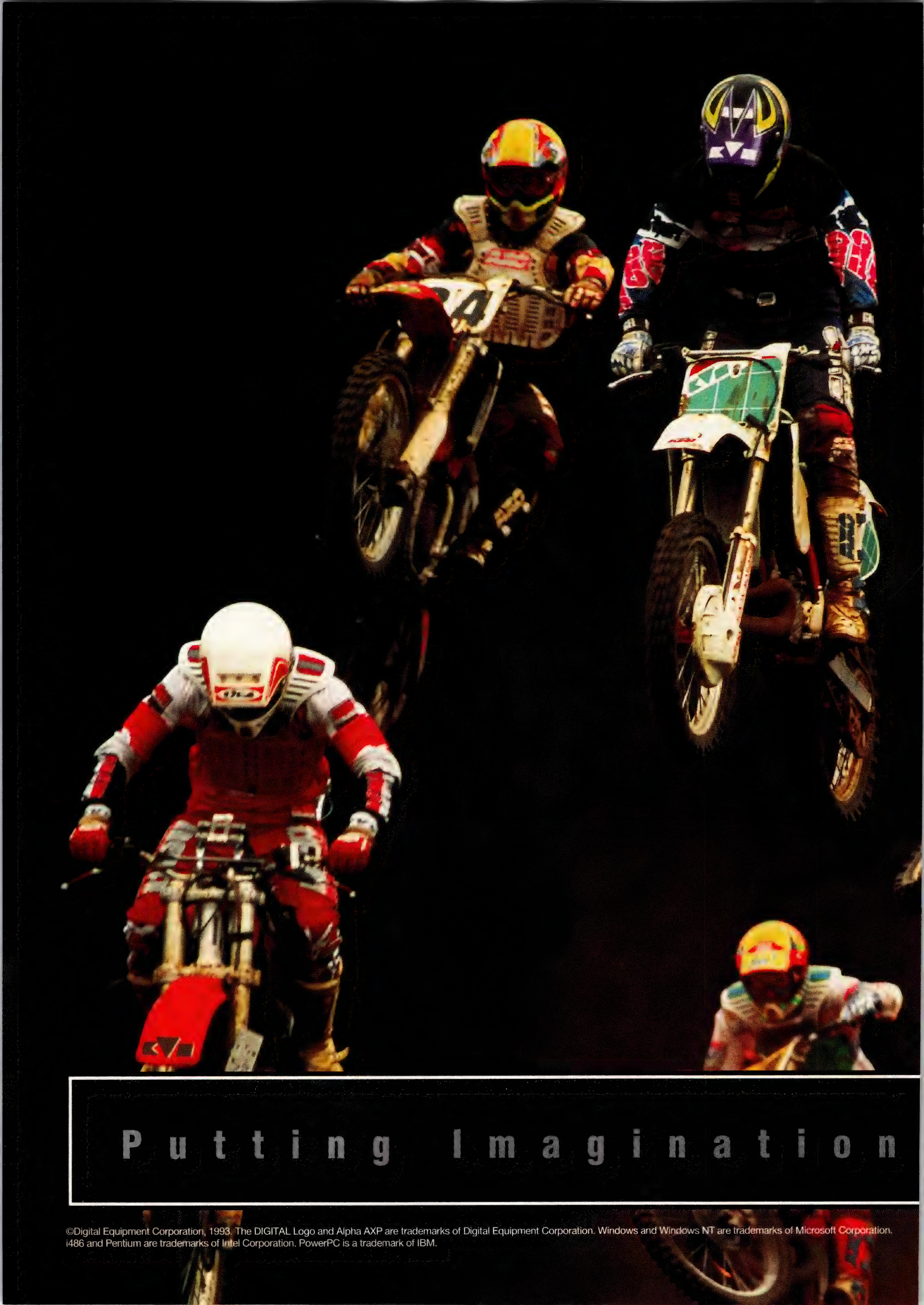

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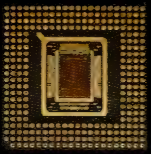

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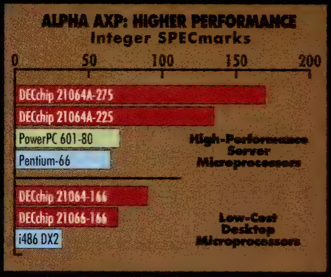

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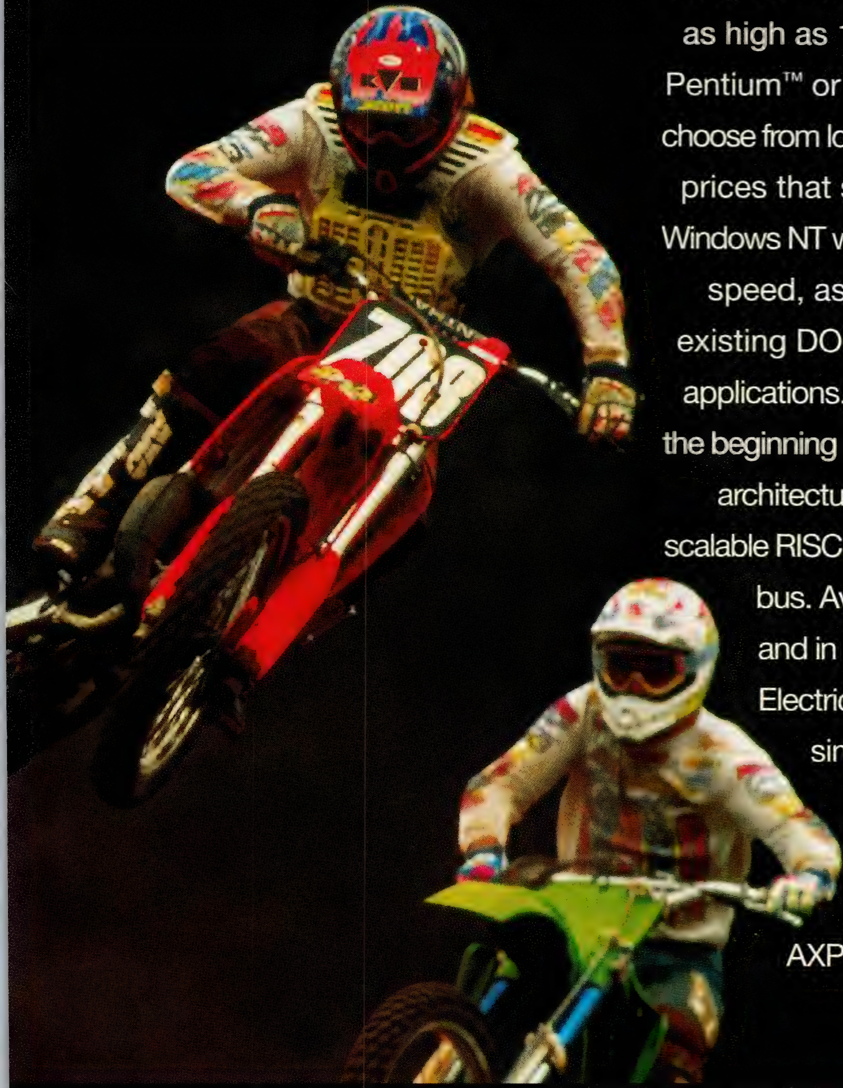

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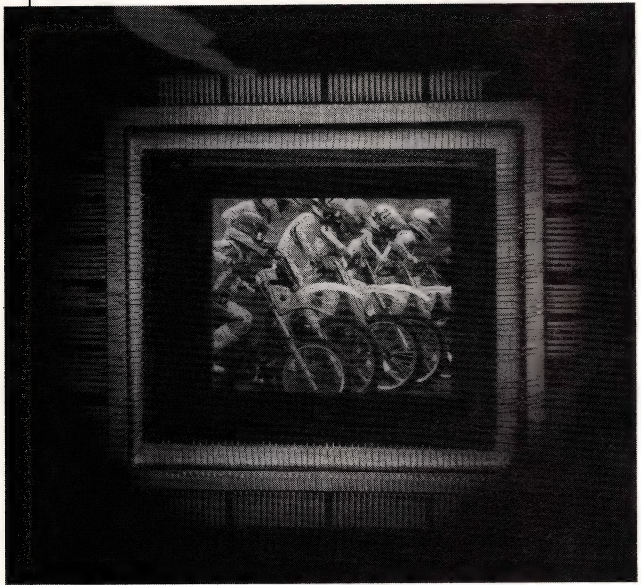

5. MOVABLE MIRRORS integrated over an SRAM form the imaging heart of a projection-TV system suitable for digital high-definition TV. The projection system comes from Texas Instruments.

germanium added to the base *(Fig. 4)*. Their all-silicon device achieved an f_t of 73 GHz, but βV_A was a low 630 V, and BV_{CEO} was 1.8 V. Devices with close to 25% germanium at the base-collector junction achieved an f_t of 113 GHz, a βV_A of 48,400 V, and a BV_{CEO} of 2.1 V.

Bellcore, Red Bank, N.J., achieved an even higher f_t of 175 GHz and a BV_{CEO} of 7.6 in an HBT (described in session 32). But this device was made from III/V materials that included InP and InGaAs.

Session 28 on high-voltage power-devices includes a discussion on the development of a 4500-V insulated-gate bipolar transistor (IGBT) that has thyristor-like performance. The IGBT was developed by a team from Toshiba Corp. Described in the same session is a power Schottky diode that cuts forward-voltage drop via trenched MOS technology. The diode was created by a team from North Carolina State University, Raleigh.

MIRROR, MIRROR...

On a somewhat different track, a TI presentation in session 15 reports on the status of TI's Digital Micromirror Device (DMD), potentially the successor to today's rear-projection large-screen TV systems. Consisting of an array of digitally controlled, integrated, movable mirrors, it offers image quality significantly superior to that available from today's projection-TV systems *(Fig. 5)*. TI built a 52-in. (diagonal) projected image display that reflects off a 0.51-by-0.39-in. (768-by-576-pixel) array of rotatable aluminum mirrors. The mirrors are integrated over a conventional SRAM chip built on a 0.8-μm twin-well CMOS process. SRAM chips are used because they're immune to photo upsets caused by light leakage into the address circuitry. The mirrors measure 16 μm across and are repeated on 17-μm centers. The DMD provides a 100:1 contrast ratio, performance competitive with the CRTs that are currently preferred for projection TVs.

The DMD is a reflective, spatial-light modulator. Each SRAM cell controls the state of rotation of its overlying mirror. A logic one in the memory cell rotates the mirror +10° while a logic zero rotates it –10°. A dark-field optical projection system converts the ±10° mirror rotations into optical on or off states. Because the mirrors' states can be switched in just 10 μs, pulse-width modulation (an analog technique) readily handles gray scale.

Three major features distinguish the DMD from other projection-TV technologies. First, the DMD provides the only all-digital solution for digital high-definition projection TVs, because the mirrors are controlled digitally by the SRAM. In conventional approaches, analog signals control CRTs and LCDs. And in digital systems, the digital data must be returned to the analog domain. Second, the DMD uses light more efficiently when compared to an LCD. Just one DMD and a rotating color wheel (shades of the original RCA proposal for compatible color TV forty years ago) achieves brightness parity with projection TVs based on three-tube-CRT and three-chip-LCD systems. The color wheel is located in the path of the light that's reflected off the SRAM-mirror chip. Finally, the DMD has the potential to become the lowest-cost projection-TV system. That's because the DMD is fabricated monolithically over a mature CMOS SRAM technology using conventional multilevel metallization techniques.

One interesting IEDM presentation is a silicon infrared (IR) focal-plane micromachined bolometer array developed by Honeywell, Bloomington, Minn., described in session 8. The device reportedly drops night-vision systems into a price range the consumer can afford *(see "Micromachined microbolometers may lead to low-cost infrared night-vision systems," p. 40)*.

NUCLEAR ALCHEMY

In terms of technology proposals, the most exciting presentation comes from the vacuum electronics arena (session 7). A team of researchers from the Los Alamos National Laboratory, Los Alamos, New Mexico, proposes to build an RF accelerator that will bombard long-lived nuclear waste, dropping the waste's half-life to about 30 years. The accelerator will require klystrons similar to those used in today's accelerator/colliders, but with unheard-of power and reliability levels. The proposed accelerator machine will need a total of 255 MW of RF power, 8.5 MW at 352 MHz and the remainder at 700 MHz. As of now, the highest-powered electron-positron collider rings, such as Tristan at KEK in Japan, develop 30 MW of RF power at 500 MHz while the LEP ring at CERN in Geneva will have 32 MW of RF power by 1995. Similar RF-generation technology can also be used in proton accelerators to produce the tritium required for nuclear weapons, effectively eliminating the need for breeder reactors.☐

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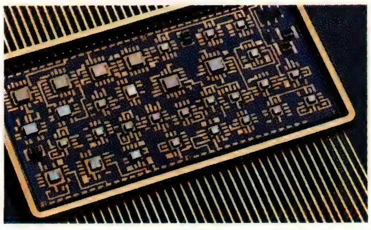

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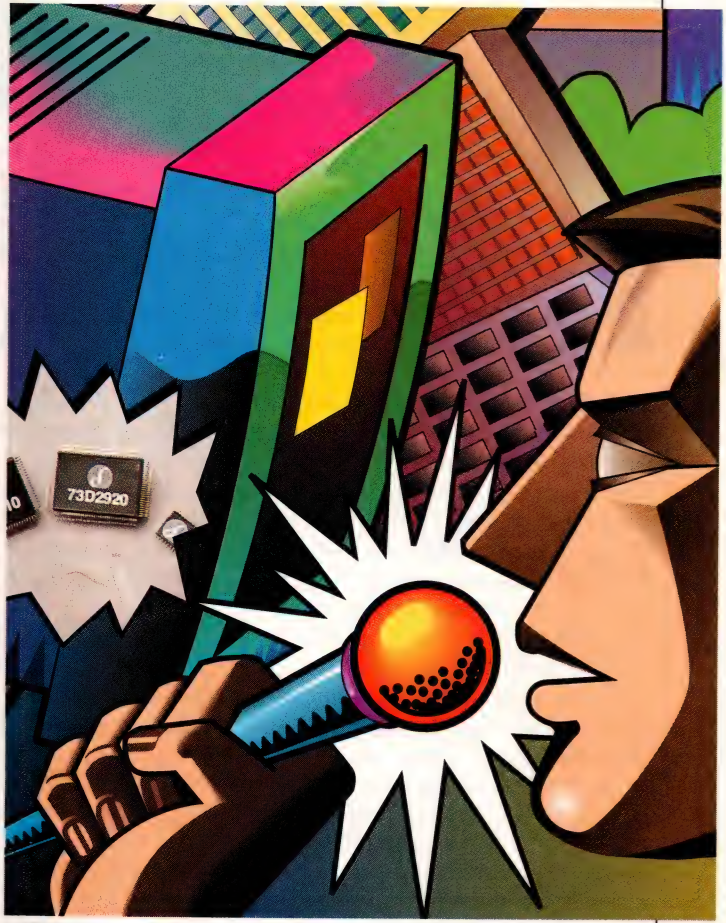
CHIP TRIO EMBODIES ALL OF THE CONTROL, DATA-PUMP, AND HYBRID FUNCTIONS FOR A V.22BIS DATA AND V.29 FAX MODEM.

FEATURE-RICH CHIP SET POWERS DATA-FAX MODEM

MILT LEONARD



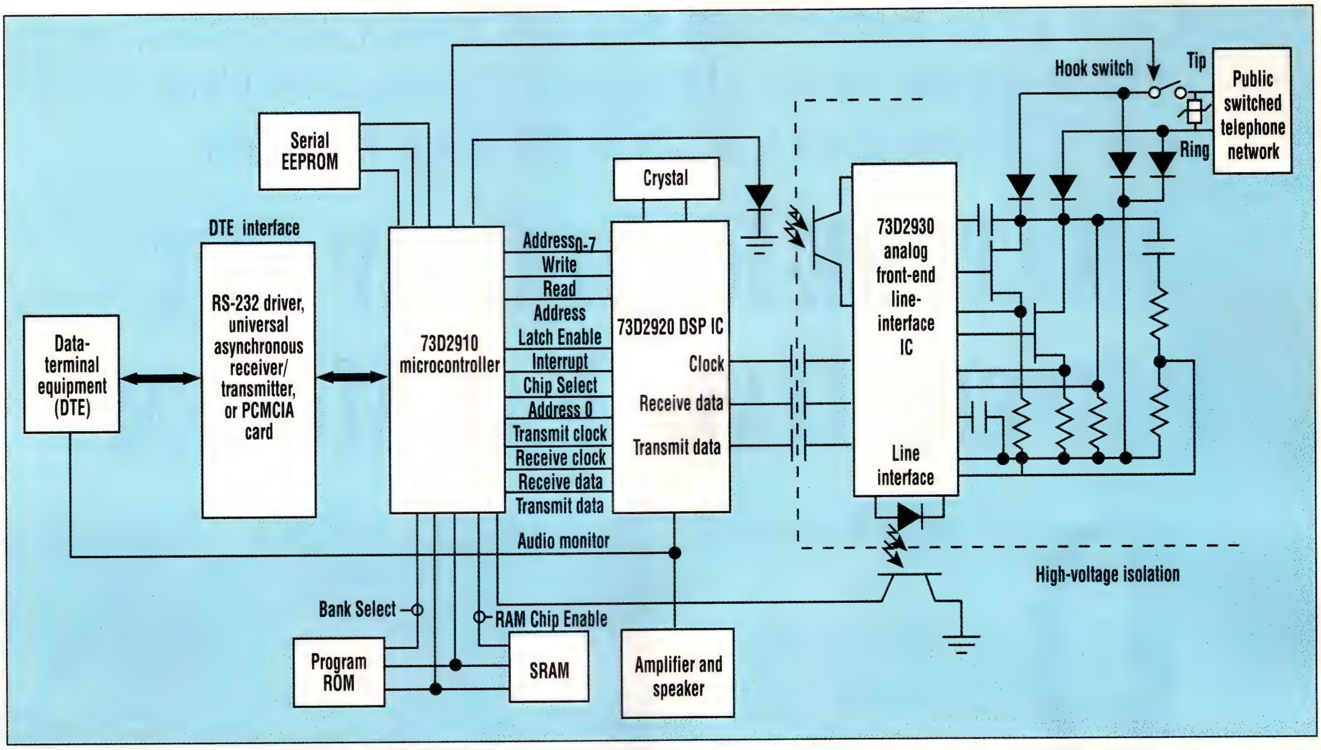
Designers of top-of-the-line data/fax modems have a number of ICs available to create high-performance machines that meet stringent international standards. However, if the design is cost-sensitive and space-constrained, such a task can be quite challenging for two reasons: A large number of expensive ICs are generally needed to do the job, and a large amount of memory is required to store quality speech.

To simplify this job, Silicon Systems Inc. came up with a data/fax chip set that makes possible cost-effective designs of data/fax modem systems incorporating answering-machine functions, sound-board capability, and voice-annotated faxes. The 73D2950T chip set can be used to create a 2400-bit/s send-and-receive modem, as well as a 9600-bit/s send-and-receive fax. The modem meets the V.22bis standard for data speed and the V.42bis/MNP-5 standard for data and error compression. The fax complies with the V.29 speed standard.

Using the TrueSpeech audio-compression algorithm developed by DSP Telecom Inc., San Jose, Calif., the chip set applies a 20:1 compression ratio to a 1-minute voice file for fitting into a storage space of only 60 kbytes, compared to 940 kbytes needed with other audio-compression algorithms. A 25-minute audio file can be stored on a single 3.5-in. floppy disk. This enables audio files to be embedded in the middle of data files for modem or fax transmission.

The 73D2950T consists of three chips: the 73D2910 microcontroller, the 73D2920 digital-signal processor (DSP) chip, and the 73D2930 analog front-end line-interface circuit (AFELIC). Fabricated with a low-power CMOS process for 3.3- and 5-V operation, the three chips make up a data/fax modem that features total power consumption of under 150 mW from the host, including external RAM, ROM, and data-access-arrangement (DAA) components.

Based on the standard 80C32 microcontroller, the 73D2910 is a custom controller containing 256 bytes of internal RAM, six and two custom standard interrupt sources, three



SEVERAL ISOLATION TECHNIQUES protect the 73D2910 microcontroller and 73D2920 data pump from high-voltage transients on the telephone line. These include optocouplers between the microcontroller and the 73D2930 analog front-end line-interface circuit (AFELIC), capacitive coupling between the data pump and the AFELIC, and a high-voltage analog optical switch in the AFELIC output. A patented capacitor circuit in the AFELIC output replaces the transformer used in a conventional data-access arrangement.

timers, an HLDC (high-speed data-link controller) packetizer, and a serial port that supports in-band (XON/XOFF) or out-of-band (CTS/RTS) data-flow control. The port, which includes a serial CMOS level-inverted EIA-232/V.24-compatible interface, connects to the host data terminal or computer and features autobaud capability from 300 bits/s to 19.2 kbits/s. Users may optionally interface the port to the host through EIA-232/V.24 drivers, a universal asynchronous receiver/transmitter (UART), or a PCMCIA card *(see the figure).*

The controller also interfaces with three types of external memory: a 32-kword-by-8-bit buffer SRAM for all data and fax modes, a 128-kword-by 8-bit program ROM, and an optional 4-kword-by-1-bit serial EEPROM to store configuration parameters and telephone numbers. Controller I/O pins are included for software control of optional LED indicators. The pins also allow a DIP switch to set up a "dumb" mode that disables fax-machine operation.

An automatic power-down mode through a watchdog timer places the chip set in an idle mode. The modem will also accept a request to power down from the host data-terminal equipment. Command and configuration of the modem is provided by an AT command interpreter that's Hayes-compatible.

DATA-PUMP FUNCTIONS

The microcontroller communicates with the 73D2920 DSP chip through an 8-bit data bus, as well as control lines. The DSP chip performs the bulk of the signal-processing operations and supports several signal-modulation schemes.

Microcontroller firmware provides access to the DSP circuit through memory-mapped registers to control functions like modulation and speed. The controller can also upload and download DSP data memory to handle such areas as the transmission level and single- and dual-tone generation. The controller can also handle the bandwidth for call-progress detection.

The 73D2920's interface register set includes a register that defines the handshake procedures allowed during the connection phase of a communications session. When negotiating a connection, the modem attempts to connect at the highest speed (V.22bis) first, but will fall back to lower speeds until a connection is secured.

For quad amplitude modulation (QAM), the chip encodes incoming data into quad bits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the band-limited telephone network. A modulator transmits this encoded data using either a 1200-Hz (originate mode) or a 2400-Hz (answer mode) carrier. The procedure is reversed using a demodulator, which also recovers the data clock from the incoming signal. Adaptive equalization compensates for varying line conditions by automatically changing filter parameters.

DSP MODULATION

In the differential phase-shift-keying (DPSK) mode, the DSP chip modulates a serial bit stream into di-bit

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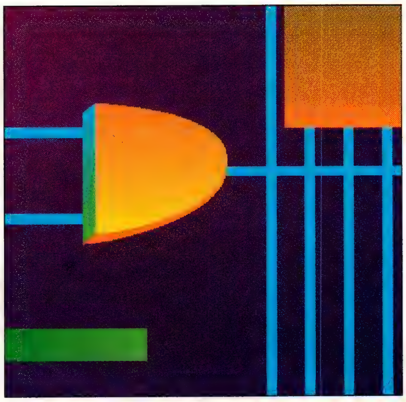

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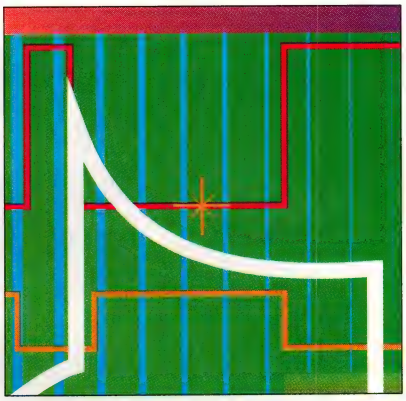

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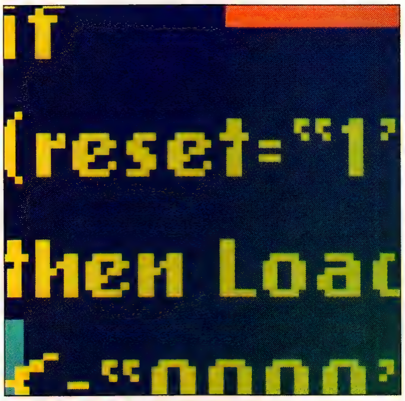

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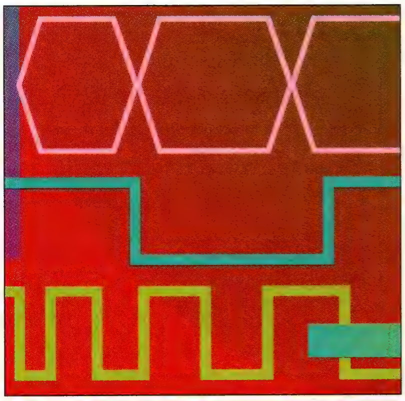

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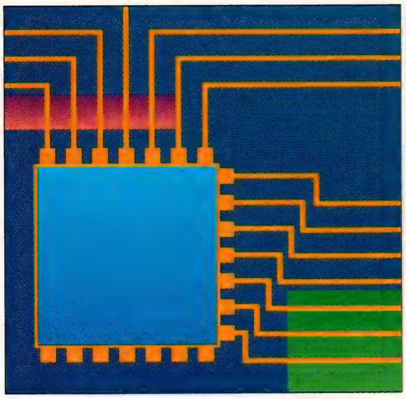

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pairs that are represented by four possible phase shifts, as prescribed by the Bell 212A/V.22 standards. After filtering, the baseband signal is transmitted on either a 1200- or 2400-Hz carrier. Demodulation decodes an incoming analog signal into dibits, converts it into a serial bit stream, and recovers the clock, which was encoded into the analog signal during modulation. Demodulation also uses either a 1200-Hz carrier (answer mode or originate analog-loopback mode) or a 2400-Hz carrier (originate mode or analog-loopback answer mode). Adaptive equalization is likewise used in DPSK modes.

Frequency-shift-keyed (FSK) modulation produces a frequency-modulated analog signal that employs two discrete frequencies to represent binary data. The Bell 103 standard frequencies used are 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space). The V.21 mode utilizes frequencies of 980 and 1180 Hz (answer mark and space) or 1650 and 1850 Hz (originate mark and space). Demodulation detects the received frequencies and converts them into the appropriate values. A rate converter circuit and a scrambler/descrambler circuit are automatically bypassed in the FSK modes.

The modem's asynchronous mode is used for communication with asynchronous terminals at data rates of 600, 1200, or 2400 bits/s. When transmitting in this mode, the serial data to the data pump passes through a rate converter that inserts or deletes stop bits. The signal then goes to a data scrambler and an analog modulator for quad-bit/di-bit encoding. Rate conversion and scrambling can be bypassed for handshaking and synchronous operations. Received data is processed in a similar manner, except that the rate converter now reinserts any deleted stop bits. Both the rate-converter as well as the data-descramble circuit are automatically bypassed in the FSK modes.

Synchronous operation is possible only in the QAM and DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a clock. No variation in the data-transfer rate is allowed. The DSP chip also includes a dual-tone, multiple-frequency (DTMF) generator that produces 16 standard tone pairs.

TELEPHONE NETWORK

By using a patented capacitor-based circuit, the 73D2930 AFELIC implements the interface to the public switched telephone network (PSTN) without employing an isolation transformer. The chip incorporates all of the necessary off-hook line-conditioning functions for connecting the modem to domestic and international PSTNs. Also provided on the AFELIC chip are a set of on-hook functions, including ring detection, loop-current-reversal detection, current sensing, and parallel-pickup detection.

The AFELIC, which typically floats on the high-voltage side of the telephone line, operates on power supplied by the PSTN. Control signals between the microcontroller and AFELIC are electrically isolated by standard optical isolators. Data bit streams between the data pump and AFELIC are modulated over a capacitively coupled interface. These attributes make the chip set suitable for compact, low-power applications, such as portable computers, PCMCIA cards, and other small battery-powered equipment.

Other AFELIC features include programmable dc current and voltage characteristics, programmable active-termination impedance, 2-to-4-wire hybrid conversion, and programmable pulse-dial "make" resistance. An integral partial-billing tone filter further minimizes modem parts count.☐

PRICE AND AVAILABILITY

Pricing for the 73D2950T data-fax chip set will be $32.50 each in OEM quantities. Without TrueSpeech, it will go for $25.00. Samples will be available in January 1994, with production quantities scheduled for late in the first quarter.

Silicon Systems, Inc., 14351 Myford Rd., Tustin, CA 92680-7022; Ed Lare, (714) 573-6000. **CIRCLE 526**

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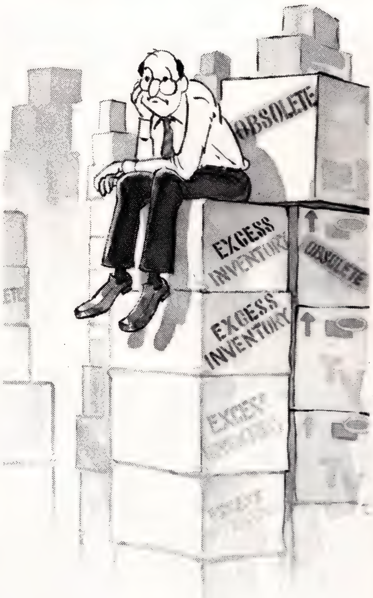

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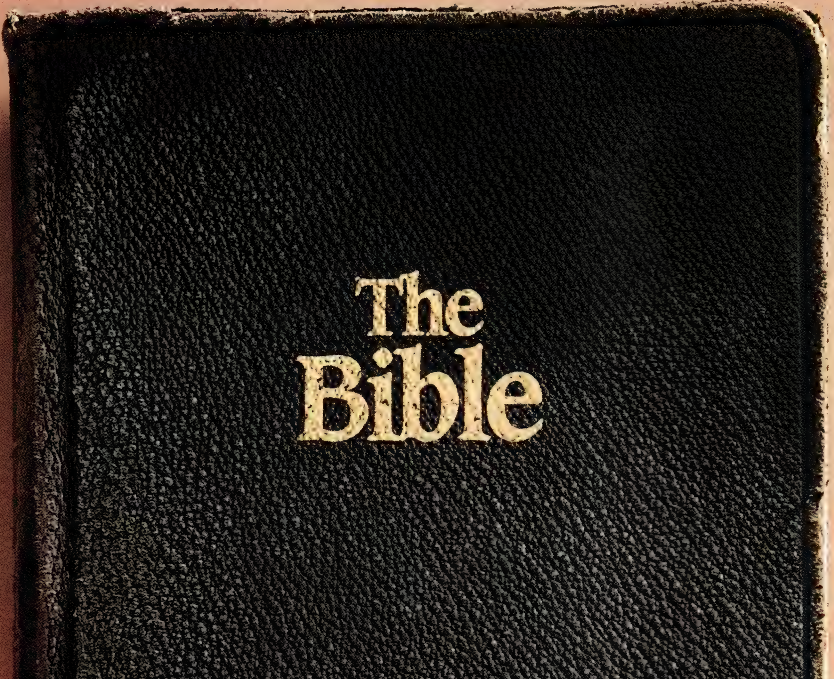

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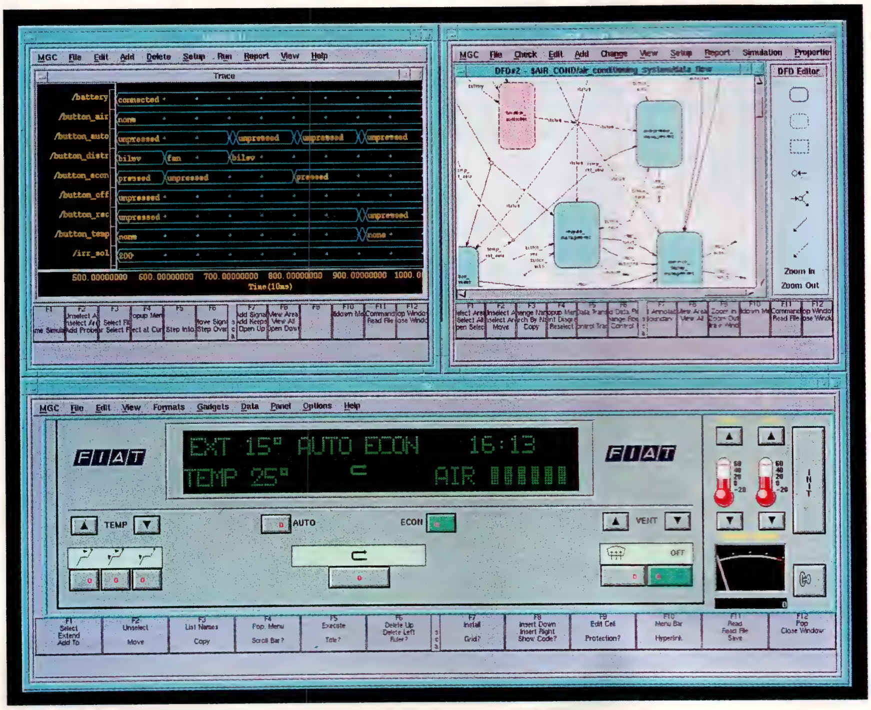

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ESDA BOOSTS CAE TECHNOLOGY TO HIGHER LEVELS

A NEW CLASS OF SYSTEM-LEVEL TOOLS PROMISES TO AUTOMATE THE FRONT END OF DESIGN.

LISA MALINIAK

Electronic system design automation (ESDA), a term that describes the automation of the design cycle's conceptual front end, promises engineering teams a new level of productivity. Theoretically, combining ESDA with existing lower-level design-automation capabilities will allow engineers to create a product on their computer without ever touching paper and pencil. But exactly what does ESDA consist of: Is it a new set of tools? Is is a new methodology? Or is it, in fact, not new at all?

Regardless of how you define ESDA, there's no mistaking that automation technology is creeping forward in the design cycle. Until recently, design tools have basically helped engineers with the logical and physical levels of hardware design, and not addressed the early phase of the product-development cycle. However, a collection of tool introductions during the past year could be described as automating the front end of the design cycle *(see "How to spot a system-level design tool," p. 66)*. These types of tools let designers explore options and trade-offs before a design is committed to hardware, software, or a combination of both. But rather than debate terminology, take a look at these tools and judge for yourself *(see the table)*.

Design-entry methods, hardware-software co-design and partitioning, and the ability to simulate and analyze a system design are three important factors for today's ESDA environments. In addition to analysis capabilities, criteria such as design optimization, hardware-description-language (HDL) generation, and user interface make a significant impact on the productivity that an ESDA tool can offer. Also, how the ESDA tool links to downstream implementation tools can affect the usefulness of the tool's results. For example, ESDA environments have limited usefulness if the product specification, partitioning, and implementation data can't be transferred to lower-level tools.

First off, these tools supply the user with a variety of design-entry methods. Design entry is an important part of an ESDA tool. That's be-

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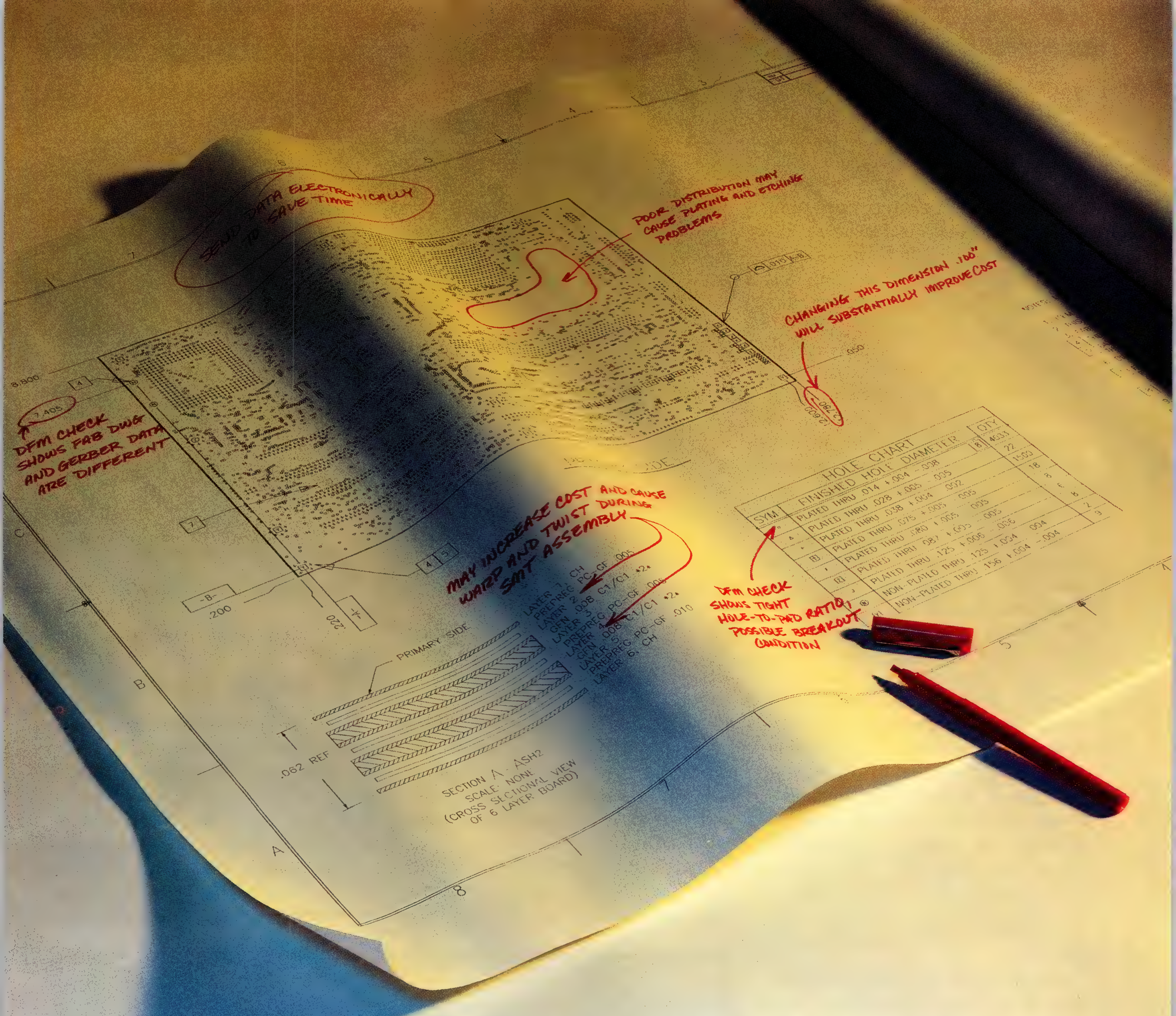
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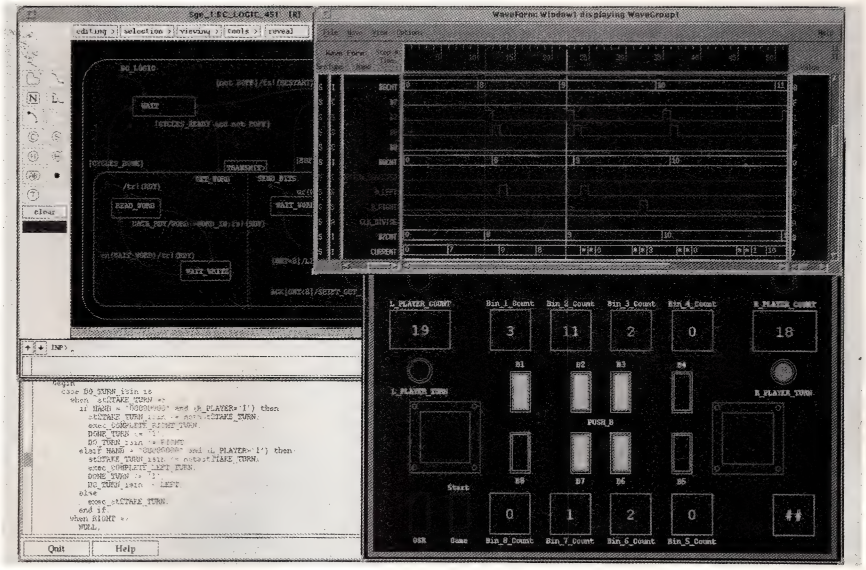


1. USERS OF THE EXPRESSV-HDL TOOL, developed by i-Logix, can represent systems with a variety of design-entry methods, such as statecharts (shown in upper left-hand window) and textual descriptions (shown in lower left-hand window).

cause at the system level, engineers need to play with concepts, which could be difficult or easy depending on how the system is described. The entry method should be intuitive so that engineers can work as they think *(see "The marriage of graphical and textual design," p. 70).*

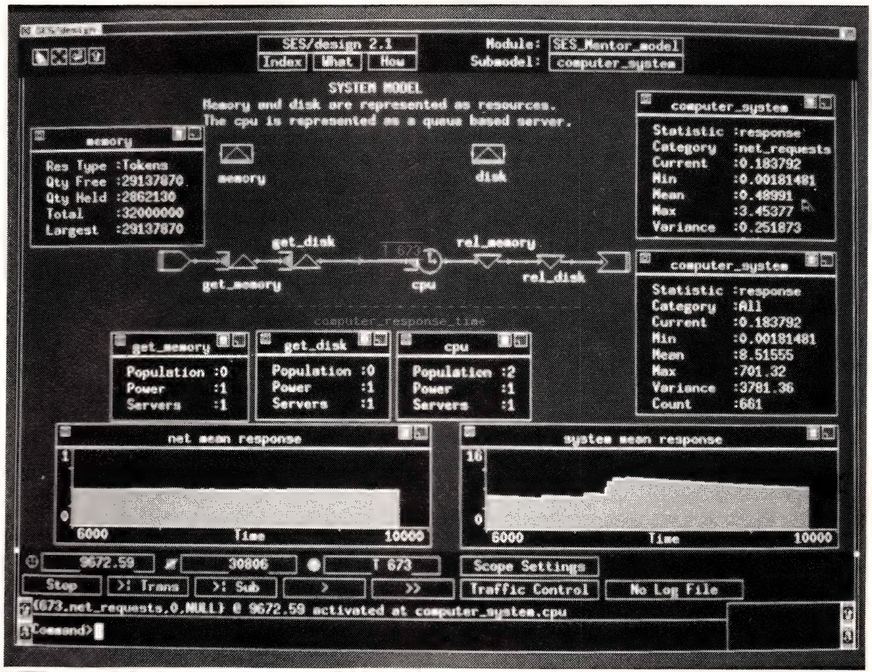
Graphical-entry methods include truth tables, state charts, and block diagrams. On the textual side, there's the VHDL and Verilog hardware description languages. In addition, some tools have options like spreadsheet-like input mechanisms.

The ExpressV-HDL tool from i-Logix provides users with graphical views that capture the architecture, functional partitioning, and functional behavior of designs *(Fig. 1).* For example, users can describe the behavior of a particular block within a design hierarchy with a "statechart," a datapath description, or a combination of statecharts and asynchronous assignments for combinatorial logic. Statecharts are created with the company's graphical language, which adds extensions to traditional state machines for describing complex behavior. These extensions include a method of describing state hierarchy and transitions between specific states throughout the hierarchy.

Design entry in SES/workbench from Scientific and Engineering Software is also done graphically. Engineers model system behavior with a graphical editor that places components in directed graphs (meaning that transactions travel in only one direction on a path). Components can be encapsulated within submodels to form higher-level components, resulting in unlimited levels of hierarchical design. The behavior of each component is specified with pop-up forms that prompt for all necessary data.

Transcend, an ESDA environment developed by TD Technologies, uses hierarchical, graphical-design entry to model a system at the highest level. A Transcend model is a network of nodes where tokens flow. Tokens can represent data, signals, and system tasks, among other elements. Nodes modify the state of these tokens and control their information flow by operating on them, storing them, or routing them. Transcend also supports multiple levels of abstraction so that users can incrementally refine the system model down to the structural level during design and partitioning.

The DesignVision software created by Vista Technologies provides a completely graphical design-entry mechanism for specifying designs at various abstraction levels, from RTL to system level. The system's behavior is partitioned into concurrent, independent sub-behaviors. Each subbehavior is a sequence of events and reactions to events called threads, which are specified using graphical primitives. Another Vista tool called



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Module:    SES_Mentor_model
Submodel:  computer_system

SYSTEM MODEL
Memory and disk are represented as resources.
The cpu is represented as a queue based server.

memory
Res Type  :Tokens
Qty Free  :29137870
Qty Held  :2862130
Total     :32000000
Largest   :29137870

computer_system
Statistic  :response
Category   :net_requests
Current    :0.183792
Min        :0.00181481
Mean       :0.48991
Max        :3.45377
Variance   :0.251873

computer_system
Statistic  :response
Category   :All
Current    :0.183792
Min        :0.00181481
Mean       :8.51555
Max        :701.32
Variance   :3781.36
Count      :661

get_memory
Population :0
Power      :1
Servers    :1

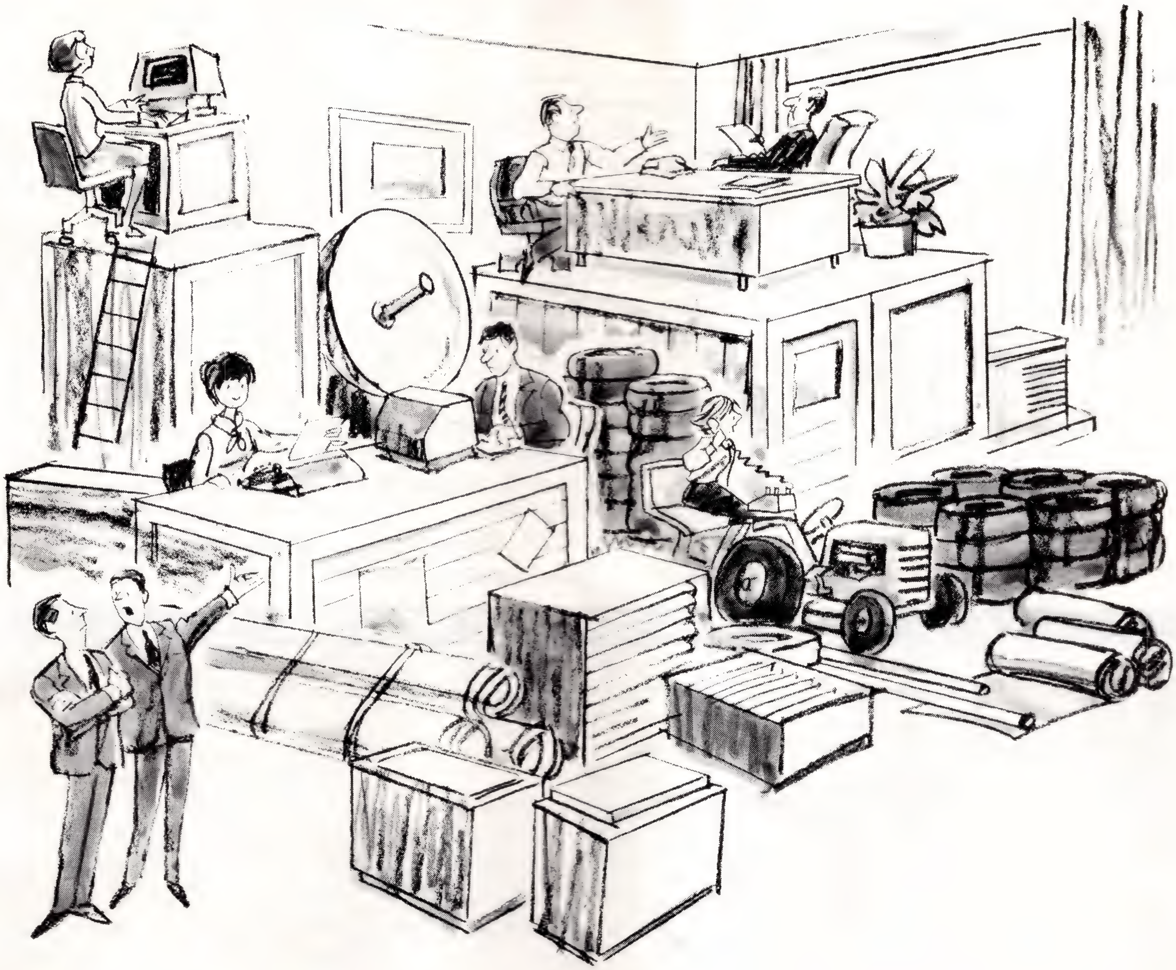
get_disk
Population :0
Power      :1
Servers    :1

cpu
Population :2
Power      :1
Servers    :1

9672.59    30806    T 673

(673.net_requests.0.NULL) @ 9672.59 activated at computer_system.cpu
Command>
```

2. A COMPUTER-SYSTEM MODEL in the SES/workbench environment consists of the memory and disk, represented as resources, and the CPU, which is denoted as a queue-based server. The graphs at the bottom of the screen plot the response times for the high-level system model.



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Model Creator models state machines and combinatorial function tables with a spreadsheet paradigm.

In the Mentor Graphics System Design Station and System Architect, data-flow diagrams, state-transition diagrams, and state matrices all provide graphical design creation and editing capabilities. These are supported by the VHDL template-driven editor for completion of detailed functionality. All are built on a central data model. A requirements editor supports the import of specification documents.

By employing Visual HDL from See Technologies, users can capture ideas and concepts with a comprehensive set of languages, four of which are graphical and one textual. The graphical languages support block diagrams, flowcharts, state diagrams, and truth tables. The textual language is VHDL.

Comdisco has three system-level design products. The Block Oriented Network Simulator (Bones) product accepts graphical-design entry, while System Design Architect (SDA) and Signal Processing WorkSystem (SPW) support both graphical- and textual-design entry.

Tools developed by Knowledge-Based Silicon (KBS) support control and datapath descriptions that are entered as text, tables, and graphics representing state machines and register-transfer models of design components. Users can specify clocking schemes, memory architecture and behavior, hierarchy, concurrency, bidirectional busing, and waveform stimulus information as part of the design description.

Finally, the design environment from Redwood Design Automation is one that doesn't currently automate graphical-design entry. It accepts designs as HDL files.

Because ESDA tools are aimed at automating the start of the design

HOW TO SPOT A SYSTEM-LEVEL DESIGN TOOL

Many attempts have been made to define the new class of system-level design tools using a simple acronym such as ESDA (electronic system design automation) and HLDA (high-level design automation). However, less work has been put into providing qualifiers and/or attributes that further clarify what such tools do differently from the current mainstream EDA tools.

Engineers are confused by this category of software because they often discover that the tools are really extensions of register-transfer-level design using hardware-description languages. Some of the systems incorporate graphics to hide or complement the HDL, or add tools like cycle simulators that are useful at the register-transfer level. But after all is said and done, the level of abstraction isn't significantly raised above today's hardware-design techniques. So, are these tools useful? Yes. But are they true system-design tools? No.

Rather than focus on another marketing buzzword, it's better to define the attributes that allow engineers to spot a true system-design tool by comparing them to non-system-level tools:

Design content
- System level: Hardware, software, mechanical
- Non-system level: Hardware-specific

Design abstraction
- System level: Architecture, algorithms, specifications
- Non-system level: Functional hardware descriptions as finite state machines, datapaths, HDLs

Capture style/libraries
- System level: Subsystems for the target application domain. Examples are: communications (modem, network, satellite); audio/video (frame buffer, image processor, speech synthesizer); control systems (actuators, sensors); automotive (shocks, suspension brakes, fuel mix); computer (CPU, memory, I/O, cache, bus arbiters)
- Non-system level: ALUs, shift registers, counters, Boolean functions

Simulation
- System level: C-based for system, algorithms, general software; HDL-based for hardware, with behavioral models
- Non-system level: HDL-based for hardware, with RTL models

Analyses
- System level: Network/transaction modeling, performance, queuing, bus contention, algorithm validation, hardware-software trade-offs
- Non-system level: Logic/event simulation, formal verification of combinatorial logic

Stimulus-response
- System level: Natural for the application domain. Examples are: communications (network traffic, modulated waveforms/eye diagrams, frequency response curve); audio/video (original, compressed, enhanced images); control systems (sensor values/actuator settings); automotive (actual road, temperature, altitude, road-salt conditions); computer (operating system, diagnostics, instruction set)
- Non-system level: 1/0, HDL, some visualization

Prototypes
- System level: Real-time software, user interface/use model virtual prototype
- Non-system level: ASIC emulation

A system-design tool works at a high enough level of abstraction to allow it to be focused on a specific application domain. It must capture, model, simulate, prototype, and view the system in an intuitive way.

Because true system-level tools are a level of abstraction away from HDL tools, they're sometimes treated as an island of automation. To maximize the leverage of the system-tool investment, cycle, they must accommodate the fact the engineering teams may not know whether a particular function will be implemented in hardware or software. It's good, then, to explore the hardware-software co-design capabilities of current products.

For example, i-Logix's ExpressV-HDL software is a part of the company's Statemate family of system-design automation tools for both hardware and software development. The Statemate approach lets users represent and validate both hardware and software behavior together in one system-level model. The graphical languages are consistent for both hardware and software design, so behavioral descriptions can be routed into either a hardware or software design environment at any point in the process. By generating HDL code or software code from the graphical system depiction, users can determine how best to partition between the two. Even late in the process, after observing synthesis or compilation results, users can reallocate functions without recapturing a design in another environment.

Similarly, modeling software with the SES/workbench product differs little from modeling hardware. The principal focus of the model is to represent the system resources and how they're used. Certain events in a system cause hardware to respond based on the status of other hardware. It's equally applicable that software drive the events and occupy the resources of a system. Software is modeled with its associated invocation time and system requirements just like hardware. Because the models are similar, the interface between them is no more difficult than in a homogeneous model. In addition, being a compiled model, SES/workbench contains another benefit: Software that can be compiled with a C calling convention can be linked into or included in the workbench model as an integral component. This encourages code reuse, and permits preexisting C-language modeling work to be utilized.

The Redwood toolset provides analysis tools, such as spreadsheets and statistical analyses, that help designers assess whether a software or hardware implementation is better. Their tools, however, don't automate that process. Hardware-software co-design (verifying that the software will run correctly on the hardware being designed) requires high simulation speed, efficient handling of large memories to store programs, and specialized tools to analyze a program as it executes. The Redwood Reveal interactor tool incorporates configurable elements called actors that can be built into hierarchies. Users create analysis and verification views from the actors that are tuned to their particular system. For instance, users can build code disassemblers, register tables, and statistical performance monitors for a Sparc processor model running a C program.

TD Technologies' Transcend addresses concurrent hardware and software design with virtual execution of embedded software on the system model. This is supported by linking actual software code and running it during the simulation. The code can be on the local platform, or on another class platform to allow for accurate performance modeling. As a result, users can optimize hardware-software partitions, optimize the location of the software, and create multiple designs with various hardware and software partitions.

THREADS AND COMPONENTS

Because the DesignVision tool from Vista Technologies uses the concept of threads and components, it allows for easy partitioning of a design into hardware and software components. For example, each concurrent software task in a system could correspond to a thread (or a group of threads). DesignVision is an open system, so users can customize its code-generation facility to create code specific to their needs. This can be used to generate software for some threads in a model, and HDL code for others. For hardware-software co-design, DesignVision can model the interaction between the hardware and software components, and the high-level behavior of the components.

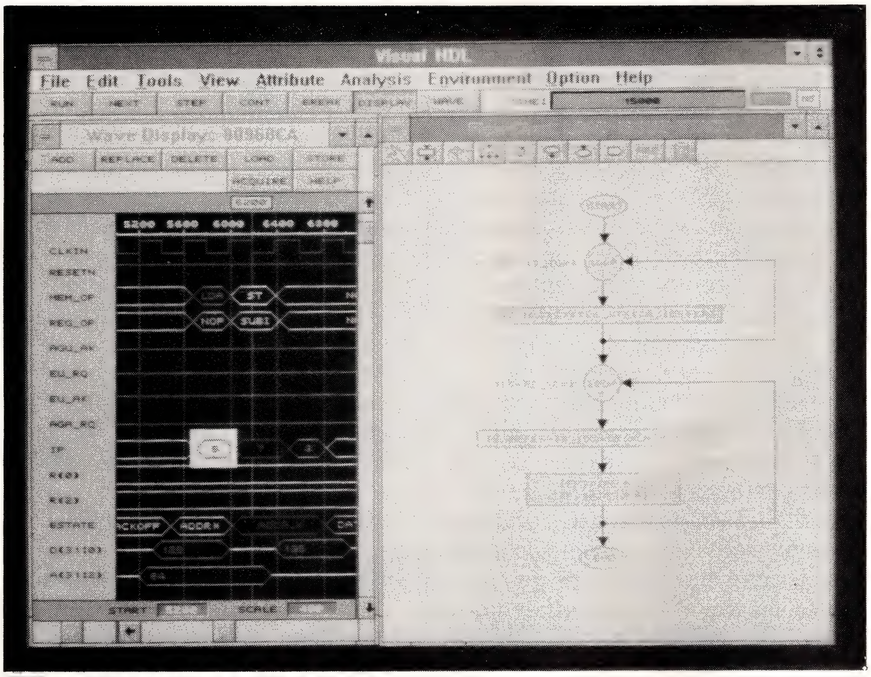
The Mentor Graphics tools contain graphical support for design partitioning, with flexible releveling and functional verifications that aid users in restructuring a design while maintaining design integrity. The dataflow diagrams support multiple levels of hierarchy and allow grouping and separating of functions to allocate toward specific implementation needs. Architectural design of both hardware and software components from requirements to full system verification helps ensure that the system is created correctly. Support for partitioning allows hardware and software functions to be allocated to the appropriate implementation tools, including special technologies such as digital signal processing (DSP).

these tools should not be considered an island, but rather a much higher level and earlier start to the EDA process. This is a very important difference because if applied correctly, they can impact the 90% of the design cost that's determined during the first 10% of the design cycle (the system design time).

Integration, however, is key to accomplishing this feat. For top-down hardware design, the outputs of the system tools can become the inputs to HDL synthesis and simulation. A simulation backplane can provide a methodology for comparing results of architectural-, RTL-, and gate-level simulations. And design and library management can help provide traceability of data from architecture to implementation.

So, regardless of what buzzword is pinned on various tools, the attributes described above can be used to determine what type of tool a product really is. Then, depending on the fit to the application domain and the functionality and EDA integration of that system tool, users can begin automating the architectural level of their design process.

Contributed by Joseph Prang, senior vice president and general manager for the System Design Group at Cadence Design Systems Inc., San Jose, Calif.


Visual HDL
File Edit Tools View Attribute Analysis Environment Option Help

3. THE VISUAL HDL TOOL designed by See Technologies incorporates a cause-and-effect feature that allows users to trace changes in signal value back to the responsible element in the appropriate graphical editor. With the logic-analyzer window, located on the left side of the screen, users can probe any signal for its value at any point of time. Then, in the source editor, users can see which state, activity box, or statement triggered that value.

Comdisco's SDA graphically partitions designs for implementation in hardware and software. The tool then automatically converts the hardware portion of the design into synthesizable VHDL for implementation. Co-design is accomplished in a variety of ways. For example, an architectural design of a programmable ASIC can be converted into a simulator model with the C-code generator. Software engineers can then write and test assembly or microcode on that model. Another example of co-design is found with simulation models of standard-part microprocessors. These models can be integrated into a design, allowing the code to run on the model and interact with the rest of the design through the chip's I/O ports.

AUTOMATIC TRANSLATION

Also from Comdisco, the SPW environment can take system block diagrams and automatically translate them into hardware in the form of VHDL, or software in the form of C or assembly code. And both system hardware and software can be modeled with the company's Bones tool. Resource models represent hardware, and block diagrams define the software jobs that interact with the hardware. For example, the effects of interrupts on a processing system can be modeled and optimized. Another example is optimizing a server's design on a computer network. Client requests to the server can be modeled based on the software application running on the client, such as a word processor. Simulations can determine when the server bottleneck changes from CPU clock speed to disk subsystem design.

Some ESDA products don't have explicit hardware-software co-design features, although they're able to handle hardware and software concepts. For example, with Visual HDL from See Technologies, users design at any level of abstraction and then verify the design's concepts. No commitment to specific implementation or to hardware-software partitioning is required.

The KBS system is generally employed when modeling hardware design elements. However, users can model software blocks as a state-machine-based algorithm using flow diagrams. Also, the company's Hydra product will support abstract-system specification, where the use of an add-on translator module will generate C code or a user-specified instruction set. This comes in handy when designers need to simulate the execution of a hardware instruction-set processor or simulate a firmware-based design.

Once a high-level system is captured and is partitioned into hardware and software, users have to be able to simulate, analyze, and verify what they've done. For ESDA environments to be effective, the associated verification tools must offer the flexibility to perform analyses and display the results in ways that are appropriate for specific application domains. For example, animation can help visualize system-simulation results.

ExpressV-HDL from i-Logix contains a pre-HDL simulator that supports design validation at the system level. For instance, it includes interactive simulation with immediate access to all design parameters, animation of graphical design models, graphical product mock-ups and custom simulator-interface panels, and waveform displays for interactive and batch simulation. This pre-HDL simulation helps verify the graphical-design entry, rather than simulate HDL code or a logic implementation. It doesn't replace the need for lower-level simulation, but rather establishes a foundation for lower-level validation by creating a functional test environment. The i-Logix products also include analyses.

ANIMATION MODE

The SES/workbench simulation operates in both the batch and animation modes. In either mode, the model can be parametrized interactively, or by using parameter files. The normal output from simulation is a report file containing statistical information about the model's performance. Typical statistics are response times for critical activities, queue lengths representing contention for resources, and custom statistics that are defined by users. In the animation mode, the progress of transactions can be monitored as they trace their execution threads through the model. An inspector window can display or graph any

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quantity in the model *(Fig. 2)*.

The simulation capabilities in the Redwood tools apply a hybrid, cycle-based algorithm. This provides the performance and capacity needed for system design, as well as debugging capabilities like stepping backwards in time, visualizing design data, and interacting directly with the design. In addition, the Redwood ESDA analysis tools explore a different set of problems than do CAE tools. At the ESDA level, designers are concerned with functional correctness, architectural implementation, hardware-software trade-offs, protocol adherence, and a host of other factors. The Reveal actors make analysis intuitive and obvious.

Transcend from TD Technologies contains a high-performance interactive transaction simulator. Specification and management of concurrency is easy—the user may specify complex triggering events and actions to be taken upon their occurrence. Events may be animated during simulation, allowing users to view the information flowing through the design. Transcend generates test stimuli algorithmically or statistically, and the system includes a set of analysis tools that perform sensitivity analysis.

Mentor's system-design tools pass off the simulation to the company's various VHDL simulators. However, during the design process, control functionality that's implement-

THE MARRIAGE OF GRAPHICAL AND TEXTUAL DESIGN

System-level design is a process of specification analysis. It requires capturing a perceived description of a system, interactively analyzing its abstract characteristics, examining how they affect the overall system performance, and then configuring appropriate hardware and software structures to form a design architecture that satisfies the requirements. At the system level, new technologies are related to architectures rather than to implementations.

Traditional tools record system specifications at the algorithm level, describing the data as mathematical or procedural transformations of the inputs. These tools don't synthesize such descriptions, but instead map a set of definitions into a specific processor.

Hardware description languages (HDLs) like VHDL give engineers a powerful tool for creating abstractions of their designs at many levels. With HDLs, engineers can define their own data types and move their descriptions far above the physical plane. For example, the homogenecus nature of VHDL's syntax and its expressive powers make it a powerful tool for describing most, if not all, system designs.

Despite the advantages, HDLs aren't used extensively. Part of the reason is that most engineers think graphically, and HDLs are textual. Some engineers resist HDLs because of their resemblance to programming. Others feel that the linear orientation of HDLs obscures the parallelism and data flow inherent in hardware. In fact, many who do use HDLs go through the step of creating the design graphically and then manually translating the design to an HDL format.

Perhaps a better approach is to provide a design methodology with which engineers can take advantage of both the benefits of HDLs and the graphics design paradigm that's more natural to them. Engineers need tools that adopt an HDL, such as VHDL or Verilog, as their primary design language, yet have a graphical representation on top of it. In other words, engineers continue to work intuitively (graphically) using block diagrams, state machine diagrams, flowcharts, or truth tables, without losing any of the power of the HDL that serves as the underlying semantics of the graphical input mechanisms. Moreover, the ideal tool should provide a mixture of graphics and text. Consequently, users can choose the methodology they feel is most productive, depending on their preferences, the design problems, and the overall requirements placed on their project.

Visual depiction of system behavior is a leading-edge method for abstract system design, making maximal use of the most intelligent and complex of the five senses. With most of today's synthesizers, an ordinary high-level description often yields overhead in code efficiency, in execution time, or in number of gates. A graphical HDL-based tool can both minimize the captured design and generate optimized code that will synthesize into faster and smaller net lists.

To truly serve electronic system design, a tool needs three fundamental capabilities. First, a design should be captured intuitively using a rich set of graphical methods, supplemented by an HDL textual entry such as VHDL or Verilog. This provides a flexible environment for engineers to express their visions without resorting to intermediate layers.

Second, this environment needs to support simulation, debugging, and refinement of the specifications at the level and form at which they were captured. Exploring and analyzing at the concept level, where the design cost is still low and the number of design objects is small, leads to a faster verification cycle.

Finally, the top-down methodology should span all phases, from specification down to HDL code generation. As a result, the tool is suitable for today's technology and for the abundance of synthesis tools on the market. Moreover, it offers a solid ground on which future environments, with more advanced synthesis tools, can be built to deal with even higher levels of abstraction.

Contributed by Elchannan Herzog, director of research and development for See Technologies Ltd., Sunnyvale, Calif., and Herzlia, Israel.

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COMPANIES OFFERING ESDA TOOLS

Company	Product(s)	Platform(s)	Pricing
Comdisco Systems Inc. Foster City, Calif. (415) 574-5800 **CIRCLE 553**	Bones: System-level tool for performance modeling and analysis of architectures SPW: Graphical tool for hardware-software design of DSP and communications systems SDA: Graphical system-level design tool for ASICs, FPGAs, and microcoded processors	Unix workstations	$12,000 and up
i-Logix Inc. Burlington, Mass. (617) 272-8090 **CIRCLE 554**	ExpressV-HDL: System-level tool that includes graphical design capture, pre-HDL simulation, design analysis, and automatic HDL code generation	Unix workstations	$32,500
Knowledge Based Silicon Corp. Columbia, S.C. (803) 779-2504 **CIRCLE 555**	flowHDL: Graphical design entry, simulation, and automatic HDL generation blockHDL: Graphical design entry and block-level partitioning Hydra: All above capabilities, plus waveform stimulus, framework backplane, and decision-support functions	PCs and Unix workstations	$5000-$25,000
Mentor Graphics Corp. Wilsonville, Ore. (503) 685-7000 **CIRCLE 556**	System Architect: Graphically represents design and generates VHDL for simulation and synthesis System Design Station: Combines the above capabilities with simulation, requirements capture, and functional visualization	Unix workstations	$34,900-$94,900
Redwood Design Automation Inc. San Jose, Calif. (408) 291-3650 **CIRCLE 557**	Reveal: An interactor tool that lets users represent simulation results in an intuitive, graphical fashion that includes animation Race: Very fast VHDL and Verilog HDL simulation that runs forwards and backwards in time	Unix workstations	$65,000
Scientific and Engineering Software Inc. Austin, Texas (512) 328-5544 **CIRCLE 558**	SES/workbench: System-level modeling tool for architectural analysis SES/vhdl: VHDL translator SES/cosim: Co-simulation with Verilog simulator	Unix workstations	$6000-$37,000
See Technologies Ltd. Sunnyvale, Calif. (408) 737-2880 **CIRCLE 559**	Visual HDL: An ESDA environment with design entry, simulation, debugging, and code generation	PCs and Unix workstations	$8000-$26,000
TD Technologies Inc. Cleveland Heights, Ohio (216) 371-9777 **CIRCLE 560**	Transcend: A graphical system-level design environment that includes an object-oriented, transaction-based tool for co-design and co-simulation of hardware and software	Unix workstations	$45,000
Vista Technologies Inc. Schaumburg, Ill. (708) 706-9300 **CIRCLE 561**	DesignVision: Graphical, event-action modeling technique for a wide variety of behavior, including system-level modeling Vista Model Creator: Spreadsheet-like interface to create truth tables and state machines that specify behavior	Unix workstations	$6000-$15,000

*All product information and pricing is provided as a guide—call the companies for exact information.

ed in state machines can be animated to check correct behavior, and full design functionality can be verified *(see opening illustration)*. Users may create test panels from the design data to provide easy, repeatable control of simulation and analysis.

With Visual HDL from See Technologies, design verification is achieved by simulating the specifications at any level of the design tree. The object-oriented simulator includes a built-in, mixed graphical-textual source-level debugger that allows users to set breakpoints, modify design objects, single-step into graphical or textual elements, trace design activities, analyze data flows, and investigate architectural interactions *(Fig. 3)*.

The simulator in the Comdisco SDA environment is a fast, clock-level simulator. In addition, the tool features analysis capabilities that are displayed through its built-in Data Analyzer. A Virtual Interface Toolset can build "virtual product interfaces" that interact with simulations. Users can then intuitively exercise designs.

Comdisco's SPW digital-signal-processing tool has a fast behavioral simulator that supports real-time interaction with the design through virtual human interfaces. Simulation can be executed on the workstation, or downloaded to a mainframe or a DSP development system. SPW's Interactive Simulation Library provides predefined analysis tools that allow users to interact with the simulation. These include a programmable function generator, spectrum analyzer, and oscilloscope. A Signal Calculator graphically creates and analyzes signals.

The company's Bones simulator is an event-driven Monte Carlo engine. A debugging environment can single-step and animate simulations. In addition, users are able to monitor data structures and bottlenecks while the simulation is executing.

The KBS flowHDL and blockHDL tools provide fast cycle-based and/or event-based simulation for functional verification and validation. Like many other system-level tool suppliers, they support interactive animation or batch-simulation modes.☐

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HIGHLY	541
MODERATELY	542
SLIGHTLY	543

CIRCLE 101

New SPICE IGBT Models

Berkeley SPICE is the most popular program for simulating the behavior of electronic circuits. One of the biggest stumbling blocks that engineers face is turning data sheet information into SPICE models that emulate real devices and run without problems. This *Simulation Idea* briefly introduces a new SPICE model for an IGBT that addresses these problems.

An IGBT is really a power MOSFET with a junction added in series with the drain. This creates a parasitic transistor driven by the MOSFET and permits increased current flow in the same die area. The sacrifice is an additional diode drop due to the extra junction and turn-off delays while carriers are swept out of this junction. The figure shows the SPICE subcircuit topology and netlist for the IRGBC40U IGBT.

The DC collector voltages, forward/reverse breakdown, nonlinear capacitance, temperature, and switching effects are all accounted for. The subcircuit values relate well to commonly available data. The figure (bottom right) shows the data book parameters and the SPICE parameters that are primarily affected by each. An application note describing the operation of the model is available by circling the reader service #.

The IGBT subcircuit was created using SpiceMod, a CAE program used for creating SPICE models from data sheets. Intusoft, the first and only SPICE vendor to provide IGBT models, also has libraries for a variety of off-the-shelf parts.

```
* IGBT SPICE Netlist
.SUBCKT IRGBC40U  71  72  74
* TERMINALS:          C   G   E
*  600 Volt  40 Amp  24.3NS  IGBT
Q1  83 81 85    QOUT
M1  81 82 83 83  MFIN L=1U W=1U
DSD 83 81  DO
DBE 85 81  DE
RC  85 71  21.1M
RE  83 73  2.11M
RG  72 82  25.5
CGE 82 83  1.42N
CGC 82 71  1P
EGD 91  0 82 81  1
VFB 93  0  0
FFB 82 81  VFB  1
CGD 92 93  1.41N
R1  92  0  1
D1  91 92  DLIM
DHV 94 93  DR
R2  91 94  1
D2  94  0  DLIM
LE  73 74  7.5N
DLV 94 95  DR 13
RLV 95  0  1
ESD 96 93  POLY(1) 83 81  19  1
MLV 95 96 93 93  SW
.MODEL SW NMOS (LEVEL=3 VTO=0 KP=5)
.MODEL QOUT PNP (IS=377F NF=1.2 BF=5.1
+ CJE=3.48N TF=24.3N XTB=1.3)
.MODEL MFIN NMOS (LEVEL=3 VMAX=400K
+ THETA=46.1M ETA=2M VTO=5.2 KP=2.12)
.MODEL DR D (IS=37.7F CJO=100P VJ=1 M=.82)
.MODEL DO D (IS=37.7F BV=600 CJO=2.07N
+ VJ=1 M=.7)
.MODEL DE  D (IS=37.7F BV=14.3 N=2)
.MODEL DLIM  D (IS=100N)
.ENDS
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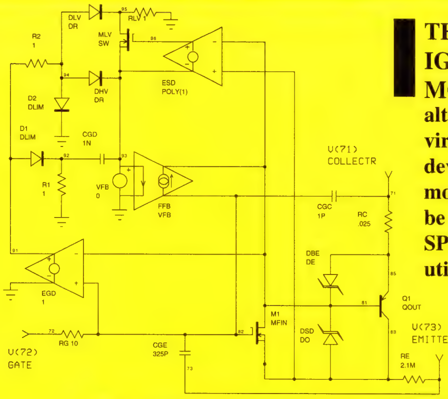
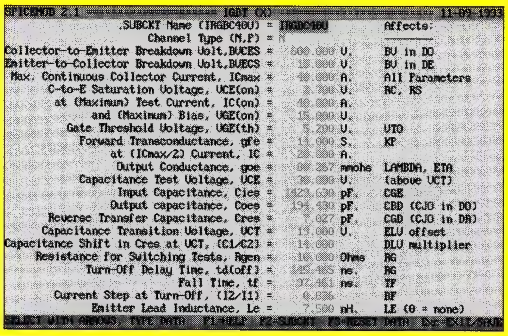


THE NEW IGBT MACRO MODEL can be altered to emulate virtually any device. New models can easily be created using a SPICE modeling utility, SpiceMod.



```
SPICEMOD 2.1 ======================= IGBT (X) ======================= 11-09-1993
                    .SUBCKT Name (IRGBC40U) = IRGBC40U              Affects:
                         Channel Type (N,P) = N                     ________
Collector-to-Emitter Breakdown Volt,BVCES =    600.000 V.     BV in DO
Emitter-to-Collector Breakdown Volt,BVECS =     15.000 V.     BV in DE
 Max. Continuous Collector Current, ICmax =     40.000 A.     All Parameters
      C-to-E Saturation Voltage, VCE(on) =      2.700 V.     RC, RS
        at (Maximum) Test Current, IC(on) =     40.000 A.
             and (Maximum) Bias, VGE(on) =     15.000 V.
          Gate Threshold Voltage, VGE(th) =      5.200 V.     VTO
           Forward Transconductance, gfe =     14.000 S.     KP
                 at (ICmax/2) Current, IC =     20.000 A.
                   Output Conductance, goe =     80.257 mmohs  LAMBDA, ETA
           Capacitance Test Voltage, VCE =     30.000 V.     (above VCT)
                    Input Capacitance, Cies =   1423.630 pF.    CGE
                  Output capacitance, Coes =    194.430 pF.    CBD (CJO in DO)
        Reverse Transfer Capacitance, Cres =      7.827 pF.    CGD (CJO in DR)
       Capacitance Transition Voltage, VCT =     13.000 V.     ELV offset
Capacitance Shift in Cres at VCT, (C1/C2) =     14.000        DLV multiplier
      Resistance for Switching Tests, Rgen =     10.000 Ohms   RG
              Turn-Off Delay Time, td(off) =    145.465 ns.    RG
                             Fall Time, tf =     97.461 ns.    TF
         Current Step at Turn-Off, (I2/I1) =      0.836        BF
              Emitter Lead Inductance, Le =      7.500 nH.    LE (0 = none)
SELECT WITH ARROWS, TYPE DATA  F1=HELP  F2=SUBCKT  F3=RESET DATA  Esc=EXIT/SAVE
```

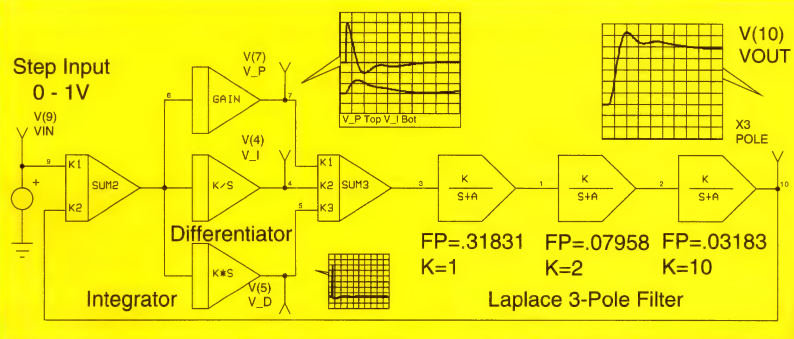
CIRCLE 102

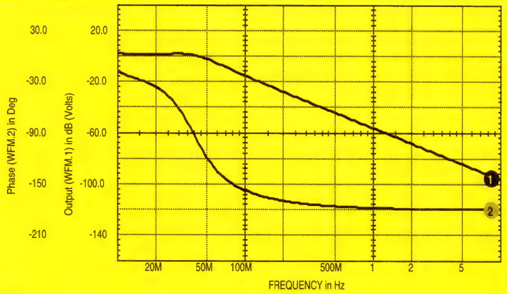
PID Control System Design

When severe requirements are placed on the precision of an automatic control process, simple proportional controllers become inadequate. In complex plants, there are often phase lags which change negative feedback into positive feedback at higher frequencies. These instabilities can be circumvented by reducing the proportional gain of the controller. However, the step response may no longer be satisfactory. As a remedy, the derivative of the control deviation can be added. This provides adequate differential gain which leads to an improved dynamic response. The steady state deviation is also a valid criteria for the quality of a control process. For this reason, the deviation can be integrated and added to the proportional and differential quantities. In this way, even the smallest deviations are summed up continuously and produce a response great enough to adjust the steady state deviation to zero.

A system using these quantities for control is called a PID control system and can easily be simulated using IsSpice's Laplace or Z transform features. The figure below shows a simple 3 pole system. The difference between the input and the output quantities is fed into gain, integral and differential blocks representing pre-made IsSpice subcircuits. The P, I, and D results are then summed and filtered through Laplace expressions; in this case a series of three generic single pole filters. Both AC and transient (step input) results are presented.

The analog computer functions in IsSpice allow it to simulate any system that can be described by a set of differential equations. This includes mixed systems containing electrical sections, described by transistors or mathematical equations, as well as mechanical and physical sections.





SIMULATION OF A PID CONTROL SYSTEM
in both the frequency and time domains.

intusoft

IDEAS FOR SIMULATION

CIRCLE 103

870MHz Class C RF Amplifier

Many designers believe that the analysis of the nonlinear characteristics of class C amplifiers is not practical with popular simulators such as SPICE. However, with the proper modeling of the RF transistors, accounting of circuits parasitics, and selection of the transient analysis options, virtually every aspect of the class C amplifier can be studied.

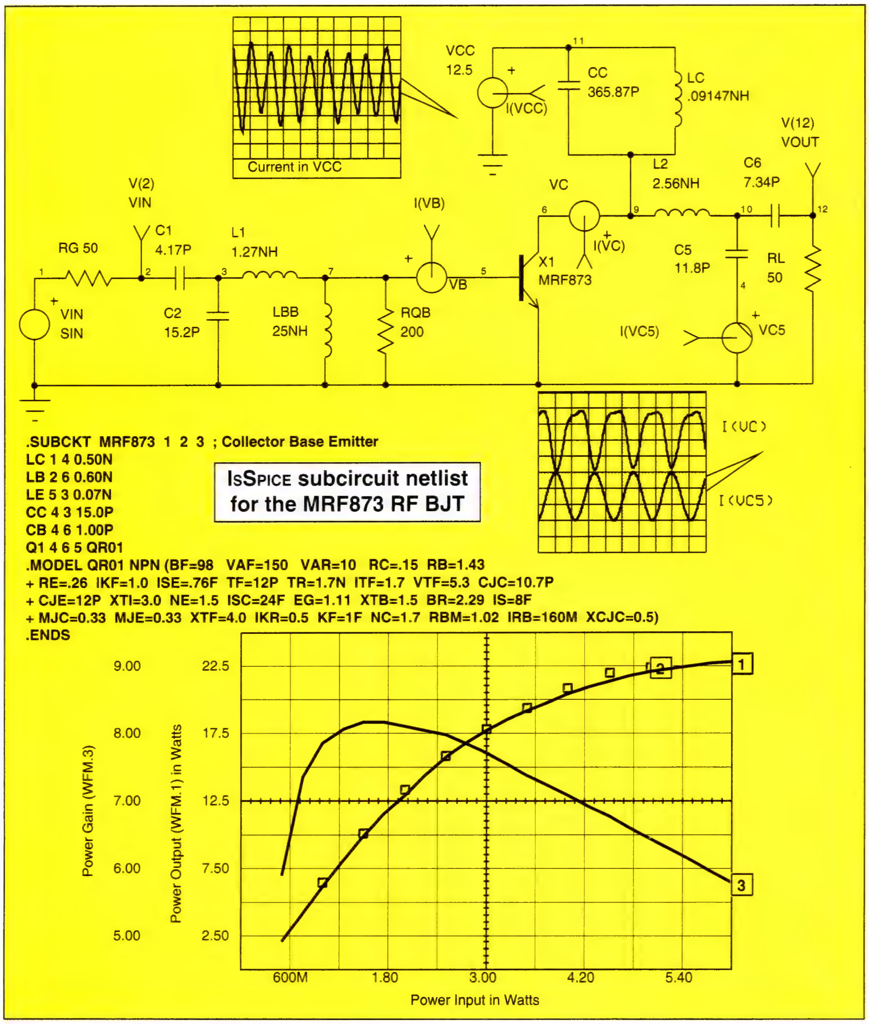
The real strength of SPICE based simulators, such as IsSpice3, is in their time domain capability where either repetitive or non-repetitive waveforms can be used as stimulus. This ability is handy for burst work, measurement of peak stresses under normal operation or momentary fault conditions, detailed study of bypass networks, and many other conditions. Since test points do not load the circuit, measurements that would be impossible on the bench can be easily made with an IsSpice3 simulation.

Shown in Figure 1 is a typical circuit used to simulate the operation of a class C power device. The device used here, X1, is the Motorola MRF873 NPN power BJT. It can produce 15 watts of output power in the 806-960MHz range. The transient simulation results required 24.6 sec. on a 486/33 (5.96s on a 60MHz Pentium) using IsSpice3, a new SPICE simulator based on Berkeley SPICE 3F.2 (PSpice®'s evaluation version 5.2 took 65.04s). At 870MHz one cycle takes about 1.1ns. Since class C circuits need some number of cycles to stabilize, the amplifier was simulated from 0ns to 20ns with output data accumulated only from 15ns to 20ns.

After initial testing of a nominal case (VCC=12.5, Power In=3W) the parameter sweeping features of IsSpice3 were used to sweep the input power. Input power is controlled by the voltage of VIN. The power gain (10*lgt(Pout/Pin)), efficiency (Pout/Pdc), and dissipation (Pout-Pdc) were all measured. Since there is no circuit loading associated with monitoring voltages and currents, measurement of the capacitor RMS current and peak voltage was possible. For nominal power input, the peak-peak voltage across C5 was 93.00V, while the RMS current was 2.082A. This type of data is vital for making informed component selection decisions.

The graph shows the excellent tracking between the IsSpice3 simulation and the data sheet values for the output power and power gain vs. input power. Other results, such as the power dissipation in the MRF873 and the efficiency and output power vs. VCC at constant input power can also be easily calculated.

From the accurate results presented here, it is clear that simulation of class C RF circuits using SPICE is practical and productive as long as the circuit and transistors are modeled properly.



IsSpice subcircuit netlist for the MRF873 RF BJT

```
.SUBCKT  MRF873  1  2  3  ; Collector Base Emitter
LC 1 4 0.50N
LB 2 6 0.60N
LE 5 3 0.07N
CC 4 3 15.0P
CB 4 6 1.00P
Q1 4 6 5 QR01
.MODEL QR01 NPN (BF=98   VAF=150   VAR=10   RC=.15  RB=1.43
+ RE=.26  IKF=1.0  ISE=.76F  TF=12P  TR=1.7N  ITF=1.7  VTF=5.3  CJC=10.7P
+ CJE=12P  XTI=3.0  NE=1.5  ISC=24F  EG=1.11  XTB=1.5  BR=2.29  IS=8F
+ MJC=0.33  MJE=0.33  XTF=4.0  IKR=0.5  KF=1F  NC=1.7  RBM=1.02  IRB=160M  XCJC=0.5)
.ENDS
```

SCHEMATIC OF AN RF AMPLIFIER running in Class C operation at 870MegHz. The schematic waveforms reveal the transient response of the currents in the power supply, transistor collector, and capacitor, C5. The graph shows the power output and power gain results. The square boxes (WFM.2) show the data sheet response for power output.

PSpice is a registered trademark of Microsim Corp.

CIRCLE 104

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CIRCLE 521

BUILD A DIGITAL TEMP MONITOR

JIM HULSEBUS
Miltope Corp., 76 Pearl St., Springfield, VT 05601.

The AD590 proportional-to-absolute-temperature (PTAT) device combined with an autoranging digital multimeter (DMM), such as Fluke's Model 77, can make a stable digital temperature-monitoring device. This holds true particularly for long distance temperature measurements, up to 100 ft.

Looking closely at the circuit *(see the figure)*, U1A forms a current-to-voltage and voltage-amplifier circuit for the total range of the AD590, –50°C to +150°C. The output of U1A then becomes the positive lead of the DMM. U1B forms a 0°C reference and calibration circuit, based upon the AD580 precision voltage reference device. This, in turn, becomes the negative lead of the DMM. The AD590 has a certain amount of calibration error, depending upon the device's grade. The 500-Ω trimmer pot removes the error at 25°C.

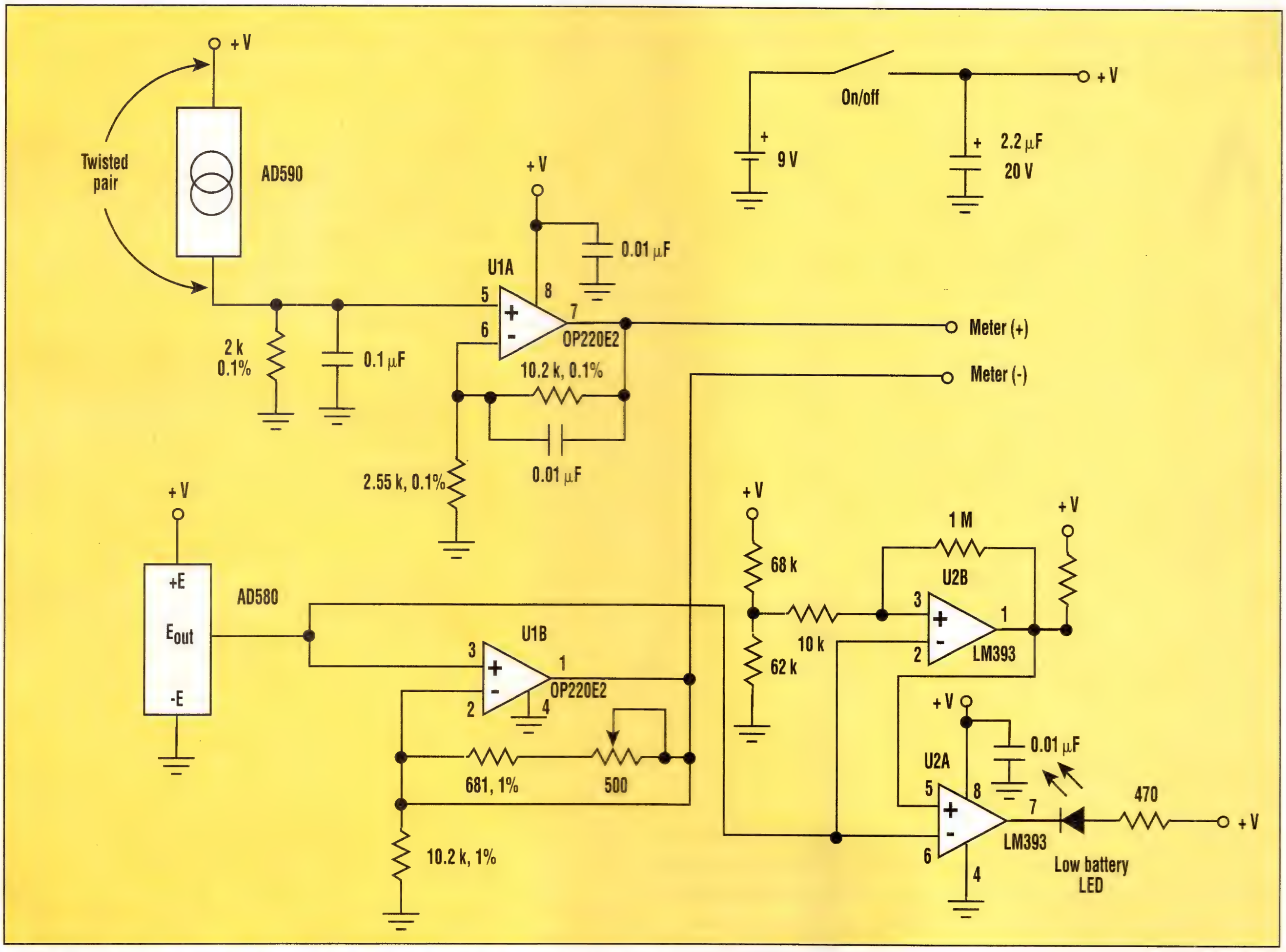
U2 is a basic comparator that forms a low battery voltage circuit. If the battery falls below 5.1 V, the LED will turn on, signaling that the battery should be replaced.

To calibrate the device, U1B's output should be set to 2.730 V (0.0°C) by adjusting the 500-Ω pot. Next, the AD590 must be attached as shown in the figure. Then, with a calibrated temperature measuring device, the 500-Ω pot should be adjusted for the correct temperature reading at 25°C. The reading on the DMM will have to be moved two decimal places to the right for final reading. For example, if the meter reads .285, the actual temperature is 28.5°C. An autoranging DMM, such as the Model 77 or an equivalent, is recommended.

The battery will last about two weeks in continuous operation. If its shut off when not operating, it will obviously last much longer.☐

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award.

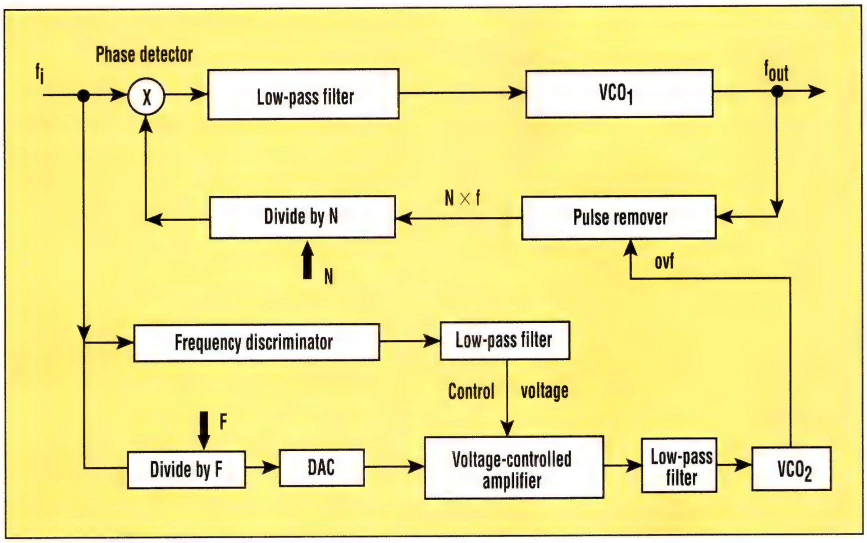


A STABLE DIGITAL TEMPERATURE MONITOR can be created by combining the AD590 proportional-to-absolute-temperature device with an autoranging DMM. It is particularly effective for long-distance measurements up to 100 ft.

CIRCLE 522

PLL SETS FRACTIONAL FREQUENCIES

NAVIN CHADDHA
EE Dept., CIS 033, Stanford University, Stanford, CA 94305; (415) 725-6029



1. THIS FRACTIONAL-N PHASE-LOCKED LOOP uses a voltage-controlled amplifier instead of a microcontroller to generate frequencies in fractional steps of the reference frequency. As a result, the total scheme is less complex and less expensive.

A fractional-N frequency synthesizer—a device that generates frequencies in steps which are fractions of the reference frequency (f_i)—will typically employ a microprocessor. Described here, however, is a fractional-N phase-locked loop (PLL) that replaces the microprocessor with a less expensive voltage-controlled amplifier and some supporting circuits. The loop is always maintained in the locked condition by changing the voltage-controlled oscillator frequency.

In the proposed scheme, the modulus control of the divide-by-N counter is implemented using a pulse remover *(Fig. 1)*. The overflow (ovf) pulse causes the pulse-removing circuit to become active, thus no input pulse is applied to the divide-by-N counter. The effect of removing the pulse is the same as if the divide-by-N counter has a division ratio of (N + 1) instead of N. To maintain the same frequency and desired phase relationship at the two phase-comparator inputs, the VCO_1 output frequency (initially N × f_i) is forced to increase by the same amount as introduced by the overflow. When the PLL system is in locked condition, the output frequency of the divide-by-N counter is the same as that of the reference. Therefore, the input frequency of the divide-by-N counter is N × f_i, and hence the output frequency of the VCO_1 (f_{out}) is Nf_i plus the ovf frequency.

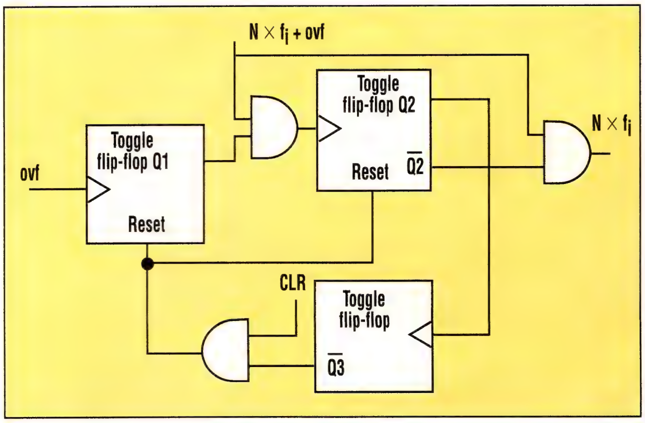
The phase-detector (PD) output modifies with the change in N or F (fractional part) input. This in turn forces a change in the output frequency of the VCO_1, whereby the divide-by-N counter's frequency is the same as that of the reference. Thereafter, the effect of the PD is to bring the phase difference between its two inputs to the initial constant value.

The ovf frequency is generated in such a way that it's the required fraction (F) of f_i. With each additional increment in the fraction F, the average value of the DAC output increases proportionally. The voltage-controlled amplifier is used to make the output voltage level correspond to f_i so that the ovf frequency generated by the low-pass filter-VCO_2 cascade is the required fraction of f_i. The frequency-to-voltage converter (frequency discriminator) followed by an LPF generates the voltage corresponding to f_i, which acts as the control voltage for the voltage-controlled amplifier.

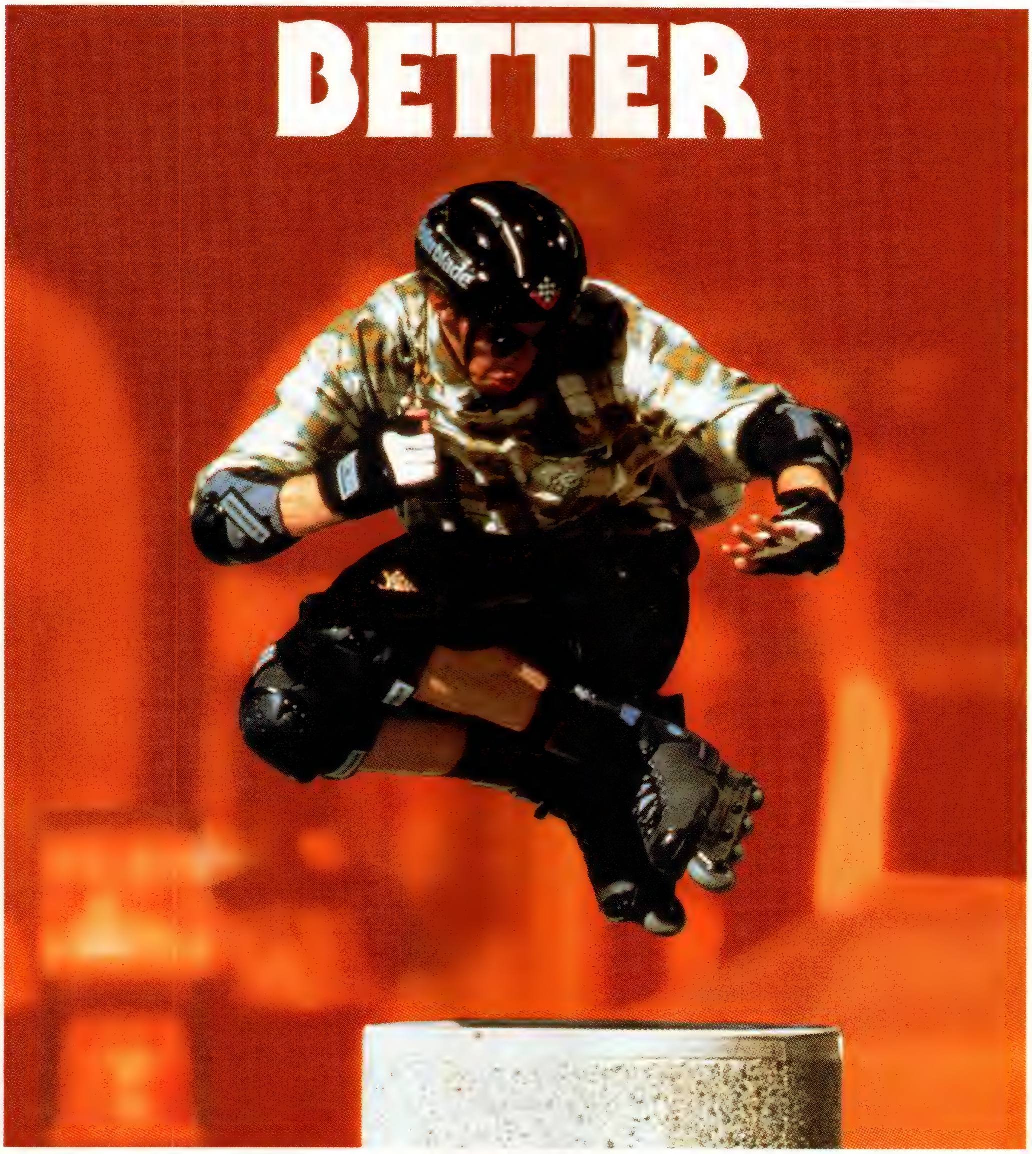
The PLL chip, CD 4046, is used to implement this scheme. It contains two phase comparators (I and II). Comparator I can lock in harmonics, whereas comparator II locks in only the fundamental. Zero phase difference is required in implementing the scheme. That's where comparator II steps in, because it can maintain zero phase difference over the entire VCO range. Comparator II, which is an edge-controlled digital memory network, works only on the positive edges of the signal and the comparator input.

The voltage-controlled amplifier is implemented using a common-emitter amplifier with a FET as its collector resistance. The FET's gate-to-source voltage thus controls the collector resistance. The pulse-remover circuit *(Fig. 2)* is implemented using negative edge-triggered JK flip-flops (7473) with reset and AND gates (7408). When clear (CLR) is low, Q1 and Q2 are low and $\overline{Q3}$ is

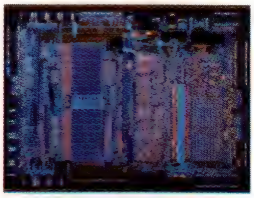
2. A pulse-remover circuit is implemented using negative edge-triggered JK flip-flops with reset and AND gates. The overflow (ovf) pulse causes the circuit to become active, therefore no input pulse is applied to the divide-by-N counter.



IT'S JUST A LITTLE BETTER



FLASH MICROCONTROLLER



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high. After removing the CLR pulse, Q1 toggles to high with the ovf's falling edge. Next Q2 toggles to high with the falling edge in the input. With $\overline{Q2}$ being low, the output is disabled. The next falling edge in the input makes Q2 toggle to low, which in turn toggles $\overline{Q3}$ to low. This resets all of the flip-flops back to the toggle mode. Therefore, $\overline{Q2}$ remains low for one complete cycle of the input, resulting in the removal of a pulse from the output.

Consequently, this scheme offers a design that doesn't require voltage compensation (at the PD output) or a microprocessor accumulator (with appropriate software to linearize the required fraction input, which would give the correct increment in ovf frequency), as is required in most present-day designs.

Instead, a frequency-discriminator-voltage-controlled amplifier-VCO combination achieves the same objective, making it less complex and less expensive. Further cost reduction can be achieved by integrating this design in chip form.☐

IFD WINNER

IFD Winner for August 5, 1993

David A. Johnson, 10198 W. Berry Dr., Littleton, CO 80127. His idea: *"Build 110-dB Beeper Circuit."*

CIRCLE

523

CONVERT SQUAREWAVE TO SAWTOOTH

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290.

The venerable sawtooth generator, also known as the ramp generator, analog time base, etc., is one of the standard building blocks in the linear designer's bag of tricks. Many implementations of this old standby exist, but most consist of an integrator, ramp reset switch, and a pulse generator to control the reset switch.

Of those, the reset pulse generator usually represents the messiest part of the design of a sawtooth generator. The lower limit of the reset pulse's duration is set by the minimum time needed to reset the integrator. At the upper end, it's limited to the longest "front porch" at the onset of the ramp that can be tolerated by the designer who's expecting a nice, sharp vertex. Usually these criteria diverge and dictate a compromise that's less than an elegant solution to either requirement.

With the circuit shown, the reset pulse issue can be avoided altogether by using a "charge pump" technique instead of the integrator reset switch *(see the figure).* S1, a CMOS SPDT switch, accepts the digital timing control signal. When the control signal is low, S1 connects the charge-pump capacitor (C_2) to the output of the integrator.

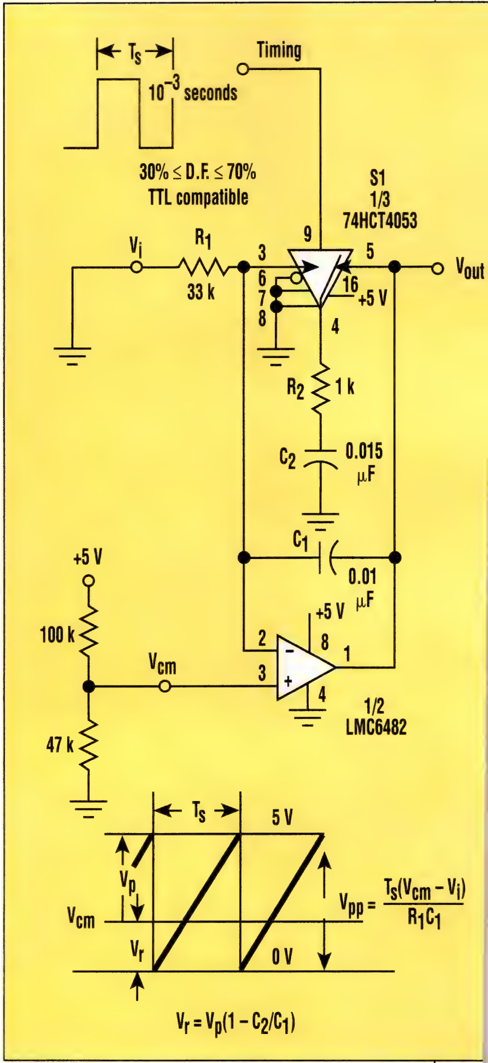
Thus, as the integrator ramps toward the peak output voltage (V_p), C_2 tracks the ramp and will hold a charge of V_pC_2 when the control signal switches. This charge will then be transferred by S1 to the integrator input, causing a reset step of $-V_pC_2/C_1$. If the duty cycle of the time control signal is anywhere near 50%, so that adequate times are allowed for the charge/discharge of C_2 through R_2 plus the on-resistance of S1, then proper operation is assured and no special conditioning of the timing signal is necessary.

Once started, the converter will converge rapidly over a few cycles of operation to a steady state where the reset step V_pC_2/C_1 equals the ramp amplitude: $T_s(V_{cm} - V_1)/R_1C_1$. This convergence will be successful provided that the condition $C_2 < 2C_1$ is satisfied.

If, for example, $C_2 = C_1$, then V_p will equal the ramp amplitude. That will cause reset to drive the sawtooth voltage to V_{cm}.

Much of the versatility of this converter, however, results from what happens if C_2 is made different from C_1. The reset voltage of the sawtooth is given by $V_r = V_p(1 - C_2/C_1)$. So, by properly selecting the C_2/C_1 ratio, the sawtooth's baseline can be moved about easily over a wide range. In the example circuit, this feature is used to generate a rail-to-rail ramp, which is usually hard to do with a single amplifier.

Note that R_2 should be chosen to limit the reset current peak to a reasonable value, and that V_{cm}-V_i input voltages of either polarity work equally well.☐



THIS SQUAREWAVE-TO-sawtooth converter can avoid the difficulties associated with the reset pulse by using a charge-pump technique instead of the integrator reset switch.

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Mike Quinlan, Chairman, CEO McDonald's (left)

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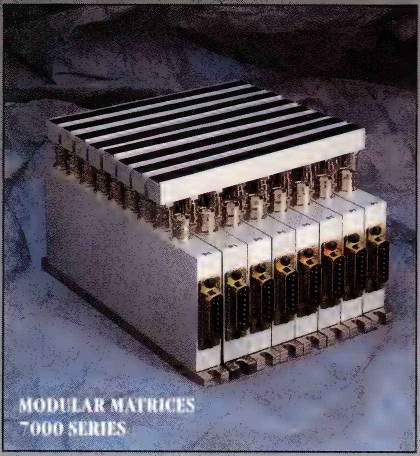

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ELECTRONIC DESIGN

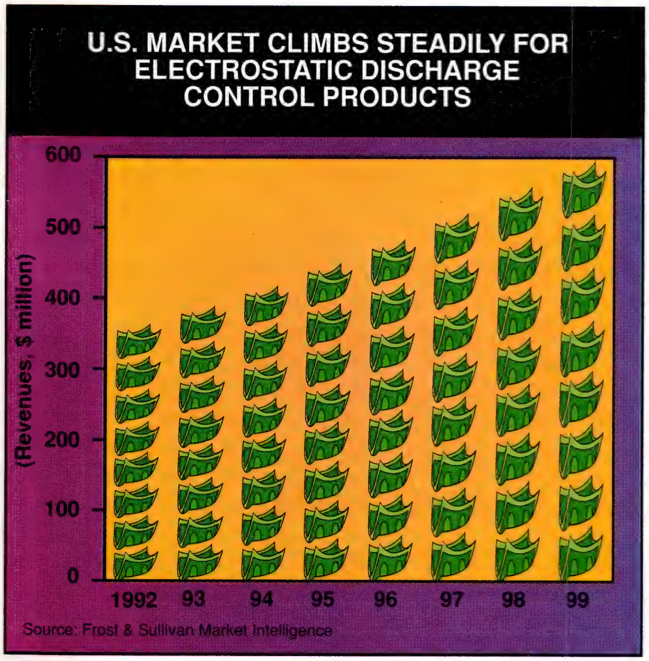
QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

A maturing electronics industry and the recession have forced makers of electrostatic discharge control products to pursue new end user markets as diverse as food processing, chemicals, packaging, consumer electronics, and industrial equipment. Nevertheless, the industry mainstays, the electronics and computer segments, made up most of the revenues for ESD products last year, which amounted to $363 million. The market is expected to be worth $594 million in 1999, growing at a compound annual rate of 7%. These market projections are drawn from Frost & Sullivan Market Intelligence's recent report, *Electrostatic Discharge (ESD) Control Product Markets—Industry Shakeout: Price Wars, Emerging Applications, New Products.*

Of the total market, packaging made up 34% of revenues; workstations 25%; flooring, 20%, ionizers, 15%, and test and monitoring equipment, 6%. The Mountain View, Calif., market research company predicts that permanent floor systems will continue to grow as well as the demand for reusable and recyclable packaging products. Also look for growth in self-monitoring, self-testing, and continuous monitoring ESD equipment and in ESD control materials like clamshells and corrugated fiberboard.


U.S. MARKET CLIMBS STEADILY FOR ELECTROSTATIC DISCHARGE CONTROL PRODUCTS

Source: Frost & Sullivan Market Intelligence

QUICK NEWS: YOUR CAREER

Your suppliers can help you improve your job performance and increase your job satisfaction. Here are some tips for enlisting their support. The advice comes from a new training process being taught to employees of major organizations throughout the nation. The process, called Peer Coaching, was created by Blessing/White, Princeton, N. J.:

- Meet regularly with your suppliers to be sure they understand your needs and ask them to suggest different ways to meet them.
- Ask the suppliers to educate you about *all* their capabilities. Learn what they do for organizations like yours.
- Hold three-way meetings between you, a supplier, and a customer to discuss how the supplier can better meet customer needs.
- Rather than tell suppliers how to do the job, explain your needs clearly and challenge them to be creative in meeting them.
- Ask your suppliers if any barriers are preventing them from giving you excellent service, and deal with those barriers.
- Focus on problem-solving, not on placing blame. Be demanding *and* understanding.

Between one third and one half of the 1.4 million managers who were laid off in the past five years will be rehired by their employers. So states Craig Dreilinger, a clinical psychologist who heads The Dreiford Group, Bethesda, Md., a consulting firm that's working with 30 companies on downsizing and its aftereffects.

"Senior executives are admitting they made a mistake to cut to the bone" he adds. "They're bringing many of their managers back as consultants."

Managers who return as consultants are sometimes paid more than they earned before and this causes resentment by the employees who survived the downsizing, Dreilinger states. The resentment can be acute when the returning managers have more power than the survivors do.

Dreilinger advises that returning managers and surviving employees meet quickly in a forum that allows both groups to admit the situation is awkward and try to reestablish relationships. Unless this is done, he adds, the survivors will be unproductive and even engage in subtle sabotage.

An early retirement offer often signals that your employer will be downsizing. Subsequent offers are rarely more attractive. Given these circumstances, you're usually better off taking the first offer.

This advice also comes from Dreilinger, of The Dreiford Group, Bethesda, Md. Companies that are downsizing usually continue to do so, he says. For one thing, downsizings often are mismanaged. For another, good leaders often leave early. Downsizing will continue for another 10 to 20 years in America.

Employers are likely to be more generous with early retirement offers at the beginning of a downsizing because they feel lots of guilt. When thousands begin to get fired, you might assume the guilt grows, he adds, but that's not the case.

EYE ON ISO 9000

Linear Technology's Milpitas, Calif., facility has been certified compliant with ISO 9001, which covers the company's design, manufacturing, and service organizations. The company's products include operational, instrumentation and audio amplifiers, voltage regulators, references, comparators, converters, switched-capacitor filters, communication interface circuits; and one-chip data-acquisition circuits. Contact the Marketing Communications Manager, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487.
CIRCLE 490

The Columbus, Nebraska plant of Dale Electronics Inc., a unit of Vishay Electronic Components, U. S., has received registration to ISO 9001 for wirewound resistors and information displays. Vishay Electronic Components is part of Vishay Intertechnology Inc. The Malvern, Pa.-based company produces resistors, resistive sensors, and other passive electronic components. Contact Greg Mefford, Dale Electronics Inc., 1122 23rd St., P. O. Box 609, Columbus, NE 68602-0609. CIRCLE 491

Chomerics Inc. has been certified to ISO 9001 for the design, manufacture, and sale of EMI/RFI shielding products in its Woburn, Mass. facility. Chomerics also produces conductive elastomers, conductive adhesives and coatings, EMI shielding, thermal management products. The Woburn, Mass., company is a subsidiary of Grace Co. Contact Norman J. Quesnel, Marketing Communications Director, Chomerics Inc., 77 Dragon Ct., Woburn, MA 01888; (617) 935-4859; fax 932-1945.
CIRCLE 492

The Espoo, Finland, facility of Planar Systems Inc., has been certified to ISO 9001 for electroluminescent (EL) flat-panel displays. The company, based in Beaverton, Ore., designs, manufactures, and markets AC thin-film EL displays and system components. Contact Planar Systems Inc., 1400 NW Compton Dr., Beaverton, OR 97006; (503) 690-1100; fax -1244. CIRCLE 493

Burr-Brown Corp., of Tucson, Ariz., has received certification to ISO 9001 in the U. S. and Europe. The company produces linear ICs, data-collection systems, and personal computer instrumentation. Contact Burr-Brown Corp., P. O. Box 11400, Tucson, AZ 85734; (602) 746-1111; fax 889-1510. CIRCLE 494

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

New product development efforts taking twice as long as expected is a familiar scenario within companies with low time-to-market sensitivity. In some work environments, engineers and their managers take pride in being able to get products to market within twice the time they initially scheduled.

Development teams wind up in this state by one of two paths. In the first route, they can understaff the effort by 50% so it takes twice as long. Or viewed another way, for a given staff level, the development team takes on twice the amount of work that can be done in the time interval. Either view produces the same result—the product gets to market late.

An important question to consider is what is the cost associated with development time taking twice as long in a highly competitive situation?

Using the model developed in prior columns, the on-time development time, r, and the delayed development time, d, become equal when development time doubles. It then becomes necessary to develop a few numbers about the scenario. What is the value of the market window, w; the value of the on-time development time, r; the value of rise-time to and fall-time from mature on-time entry sales, a; and the value of the rise-time to and fall-time from late entry sales, b?

Example 1: 12 months' development time with a 24-month market window with rise and fall times equal to 6 months.

r	S	d	w	a	b	Profit ratio
12	1	0	24	6	6	0.00
12	0.5	12	24	6	6	0.64

A 50% understaffing results in the loss of 64% of profits! New product development organizations serving workstation and minicomputer markets should not be surprised with these results.

Example 2: 9 months' development time with a 12-month market window, with rise and fall time equal to 3 months.

r	S	d	w	a	b	Profit ratio
9	1	0	12	3	3	0.00
9	0.5	9	12	3	3	0.86

Taking twice as long under this scenario cuts lifetime profits by 86%! Companies introducing Intel and Motorola developments into the marketplace and disk drive developers often times perform in this area.

These simple calculations can be augmented by more detailed financial analysis techniques. For those interested in greater detail, I suggest setting up a cash flow scenario where monthly development costs follow the staffing profile and where monthly profits follow the profit profile. With the profiles set on a spreadsheet, look at IRR, the return factor, and the return on sales. All these numbers will be bad!

The main point to be derived from this column is that you cannot consistently miss the staffing ratio by a factor of 2 and expect to remain in business. Managers, engineers, and support staff must learn how to accurately estimate and sequence the work load so that the right number of resources are assigned to get the job done on time.

More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.

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PLCC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP
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CIRCLE 201 FOR U.S. RESPONSE

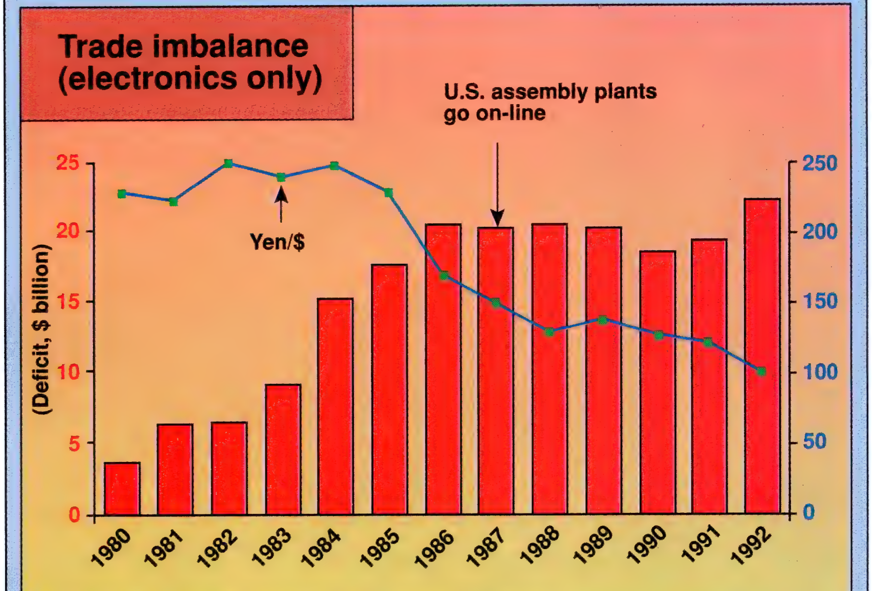
CIRCLE 202 FOR RESPONSE OUTSIDE THE U.S.

TALES FROM A SKUNK WORKS

If it is true that cold war has turned to economic war, what rules and what scoreboards are used? How can you tell if your nation, company, division, or skunk works is winning or losing? Keeping score is a problem. A fatal mistake in war is focus on the wrong things. Remember the "body counts" during Vietnam? The adversary considered body counts or battles irrelevant. Stock prices (earnings) are as irrelevant to global trade as body counts were to Vietnam. Misguided objectives make it easy for an opponent to prevail. For example, U. S. firms predictably fled lucrative, growing, consumer electronics markets rather than endure low earnings.

A better scoreboard than Wall Street is trade balance and currency strength. With exceptions and despite good stock prices, the U. S. is losing in technology-based business. The U. S. trade imbalance with Japan in electronics measures defeat. *A 250% devaluation of the dollar didn't help us export more or import less.*

Economists call this a "structural deficit" because devaluing to drop prices on goods that you don't produce—TVs, VCRs, video cameras, stereos, FAXs, CDs, and displays—is futile. Even these dismal figures mislead. The scoreboard is rigged.



Source: American Electronics Association, U.S. Department of Commerce

The trade deficit miraculously leveled, and the official numbers have since been set at $20 billion. Leveling coincided with debate in Congress about dumping and embargoes. The adjustment mechanism is local assembly plants.

These are called "screwdriver plants," because that is how value is added. A product is designed, produced, assembled, and tested offshore, but the final step, putting it in a case and the case into a box, is left for the U. S. to ease "trade friction." These products are officially U. S. goods and perhaps exports, but the plants produce few local family wage jobs. If the offshore parent prices the assemblies high, there are no domestic profits to tax.

What is the output of U. S.-sited Japanese plants, and what percentage of value is locally added? *No one knows.* We are the only major trading nation who fails to track this. One Customs Commissioner backed off on collecting tariffs from Honda after she found local content probes were career-threatening (*Business Week*, Nov. 18, 1991).

I suspect that the true deficit is more than $40 billion and growing. A difference of $20 billion represents some 200,000 jobs, the same number the Clinton administration hopes to gain from NAFTA, but better jobs.

Useful metrics for new product success are almost as elusive. My next column will discuss useful scoreboards for skunk works and new product development.

John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of High Tech with Low Risk. *To order, phone (503) 280-8547.*

QUICK NEWS: WORKSHOPS

Free workshops are being held on the IEE Inspec Database, which contains information on electronics, computing, and information technology. An introductory, all-day session is for users with a knowledge of online searching but who need more information on Inspec's coverage and content; hands-on practice is provided. An advanced all day session is intended for frequent users wishing to improve searching skills for cost-effective, accurate results. Advanced applications are covered in hands-on exercises to be held: December 13 (advanced), in Orlando, Fla.; Dec. 14 (introductory), Orlando; Dec. 16 (advanced), Tampa, Fla.; Dec. 17 (introductory), Tampa. For dates in January 1994 and beyond, contact IEEE's Service Center, IEE/Inspec Dept., 445 Hoes Lane, P. O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-5549; fax (908) 981-0027. CIRCLE 495

QUICK NEWS

During the past four years, federal laboratories have developed nearly 200 technologies related to semiconductor devices, antennas, circuits, and optoelectronic devices and systems. To learn more about these technologies and how to commercialize them, contact the National Technology Transfer Center (NTTC) at (800) 678-6882 or use NTTC's electronic bulletin board; phone number is (304) 243-2561 for low-speed modems; -2560 for high-speed modems. NTTC is an independent federal organization that helps companies commercialize technologies developed within the country's 700-plus federal labs.

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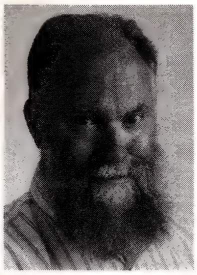
PEASE PORRIDGE



BOB'S MAILBOX

Dear Bob:

The degree vs. no-degree issue is more complicated than your readership realizes. There is great value to experience, willingness to attack a problem, and native intelligence and intuition. A person is born with some qualities, some are developed through education and training, and some can only be acquired through years of working in the real world.

The technical professions have identified a body of knowledge representing the core knowledge one must know to be proficient in that profession. The degree is a certificate indicating that the holder has acquired mastery of that core knowledge. It doesn't certify that the holder is creative, hardworking, or pleasant to be around.

The permutations of degrees, experience, native ability, and a dozen or more other qualities are what make the whole engineer. Holding a degree is only one of these qualities; it shouldn't be overrated, but on the other hand, it shouldn't be underrated either.

I have worked as a software engineer (programmer) for 23 years. I recently received a masters degree in Computer Science. The knowledge that I acquired through the masters course work would have helped relatively little in my career.

Conversely, I can now do certain kinds of analysis and development that I couldn't previously. I expect the same to be true of other technical professions.

There is no reason why a non-degreed engineer shouldn't take the time to complete a degree. Between testing out lower-level courses and credit for work experience (post fact, it's called an independent study class), it is not a large burden.

A technical course of study is focused and relevant to work. Yes, any good school will want you to jump through a few hoops, but the fact is, they will work with you to tailor a program if you work with them.

Assuming you have all the qualities that make a good professional engineer, why wouldn't you want to take the classes for a degree? You have to study continuously to keep up with new developments. So do your studying at a university where you can interact with a professor who has real expertise.

Your employer will help pay for the tuition and may even give you time off to attend classes. Time, money, value. Do you think you won't learn anything? You will certainly learn something you would not have learned just studying on your own.

With technology becoming more complex, and with the aerospace recession, certain job markets are more competitive. It may not be right, but the personnel people set standards that will prevent non-degreed individuals from being hired, and will lay off the non-degreed first.

CORY K. HAMASAKI B.A, M.S.
Alexandria, Va.

I sure agree with your first five paragraphs. But, there's "no reason" not to complete a degree? It's "not a large burden?" Hey, maybe I should steal the shoes off my baby's feet, ignore my family even more than I do, stop writing columns, and go back to school to learn how to design linear ICs from "a professor who has real expertise?"—RAP

Dear Bob:

Back in May, you put out a challenge for Fuzzy Logic applications. This is not one. In fact, all I have read indicates that F.L. designers have never heard of feedback circuits in control systems.

The examples of F.L. that I have read are one-dimensional systems: If the temperature is such, then the "comfort" parameter falls into cold/normal/hot to such and such a degree. A simple feedback controller can easily handle this kind of problem. Fuzzy Logic is overkill for an application that could be done more simply. Its only advantage is being able to make advertising claims that it's "Fuzzy Logic Controlled".

F.L. is an idiot level of Artificial Intelligence. AI can determine the correct identity or action from a complex input by using appropriate rules. The next higher level allows it to learn. The next level allows a "best guess" with incomplete data. For F.L. to shine, it must implement at least some of these principles. The degree to which a rule applies, and how it is applied, is determined by the data input. Rules modify the rules according to data. If data is missing or way out of line, fallback rules and constants may be used.

For example, F.L. that applies humidity as well as temperature would be a much more appropriate Fuzzy Logic application than a simple temperature controller. As humidity changes, the transitions between cold/comfortable/hot change position and possibly slope. At very-high humidity, the comfort zone may disappear. The controller would need to control both temperature and humidity through heaters, controllers, humidifiers, and dehumidifiers.

As long as F.L. is used in one-dimensional systems, it will flop. The more dimensions it uses, the better it will outperform other simpler feedback systems. However, the more dimensions it operates in, the more complex it becomes, and the more a true AI system may be appropriate.

I am not an expert in AI or F.L., but rather in communications systems. But I do believe that F.L. will fail until it is used to perform judgment of appropriate behavior with incomplete or complex data.

I also agree that many articles are more F.T. (Fuzzy Thinking) than Fuzzy Logic. Thanks for the breath of fresh air on F.T. (or was that F.L.?).

PAUL M. SCHUMACHER
Ademco Inc.
Syosset, N.Y.

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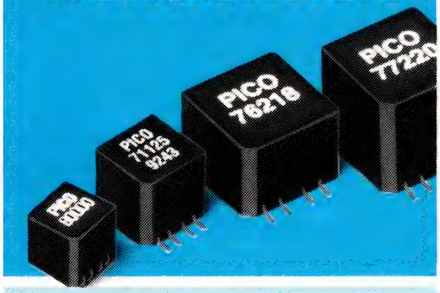

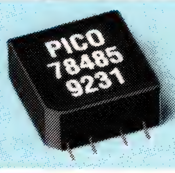

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CIRCLE 205 FOR U.S. RESPONSE
CIRCLE 206 FOR RESPONSE OUTSIDE THE U.S.

PEASE PORRIDGE

Many demonstrations of new technology are greatly simplified. But most F.L. examples give no clear explanation of what works—or why! I hope my last two columns helped clarify that.—RAP

Dear Bob:

How I have waited to catch you in an error! The large Van de Graaff generators used at most physics research labs are horizontal—not vertical as you implied in the Oct. 1 column, "What's All This ESD Stuff, Anyhow?"

I can now die a happy man. (I might want to put it off a few years, though, since I am only 33.)

CHUCK McCOWN
Data Com
Quincy, Ill.

Just like I said: Since most conveyor belts are vertical, those horizontal Van de Graaff generators are perpendicular.... I once thought I'd made an error—but that was a mistake....—RAP

Dear Bob:

I greatly enjoyed your column, "What's All This Ground Noise Stuff, Anyhow?" in the June 24 Analog Applications Special Issue. The importance of being able to make an accurate measurement can not be understated. I remember "Doc" Edgerton telling our circuit design class (circa 1955), "You guys will never be good engineers until you learn to take a measurement!" That admonition is probably truer today than it was back then, when you could almost get by measuring voltages with a wet finger and power levels with your sense of touch (or smell—depending on the degree of overload).

One statement you made in your article is more incorrect than not, and should be clarified. You say in reference to magnetic noises, "Unfortunately, copper or aluminum will not reject or attenuate these magnetic noises." If you check almost any book on EMI reduction techniques, you'll find references to attenuating ac magnetic fields with "reflective shielding" by using conductive enclosures made of those very materials.

An ac magnetic field induces a current in the shield, which creates an opposing field. I'm sure someone who remembers his/her electromagnetic field theory better than I do could derive a rigorous proof showing that ac magnetic fields are attenuated by conductive enclosures. I suspect the proof would show that even a dc magnetic field would not penetrate a completely closed box made of infinitely-conductive material. The material I've read states that reflective shielding is more effective than using magnetic materials above about 15 kHz, and the thickness of a reflective enclosure need only be about three times the skin depth of the material at the lowest frequency you're trying to attenuate. Holes for leads, adjustment tools, etc., should be kept as small as possible. Better one hole per wire than one big hole to take a whole bundle. The old "loop size" thing again.

Sometime last year I read a technical note from Hewlett-Packard that described the extremes they took to provide magnetic shielding for the front end of a wideband measuring instrument, with a multiple-layer shield that was constructed out of Mumetal for low frequencies and copper for higher frequencies.

I recently had to reduce the external 25-kHz magnetic fields produced by a small switching power supply in a spacecraft system. The 25-kHz H-field, as measured with a shielded loop antenna a few inches away from the supply, was about 20 dB over the allowable limit. I reduced these emissions over 30 dB by surrounding the supply with a cigarette-pack-size aluminum box with 1/16-in. thick walls and cover. To get maximum attenuation, I had to clamp down the cover with countless screws. An alternative would have been to use a metal mesh conductive gasket between the cover and the box, and fewer fasteners.

JEFFRY A. WISNIA
MIT 57 EE
Jeffry Wisnia and Associates
Winchester, Mass.

Thanks for correcting my ignorance. Your comments are of great value—examples of problems in the real world, indicating that these very tricky principles are not well known. Many people read my Ground Noise column, but only you wrote in to educate us!—RAP

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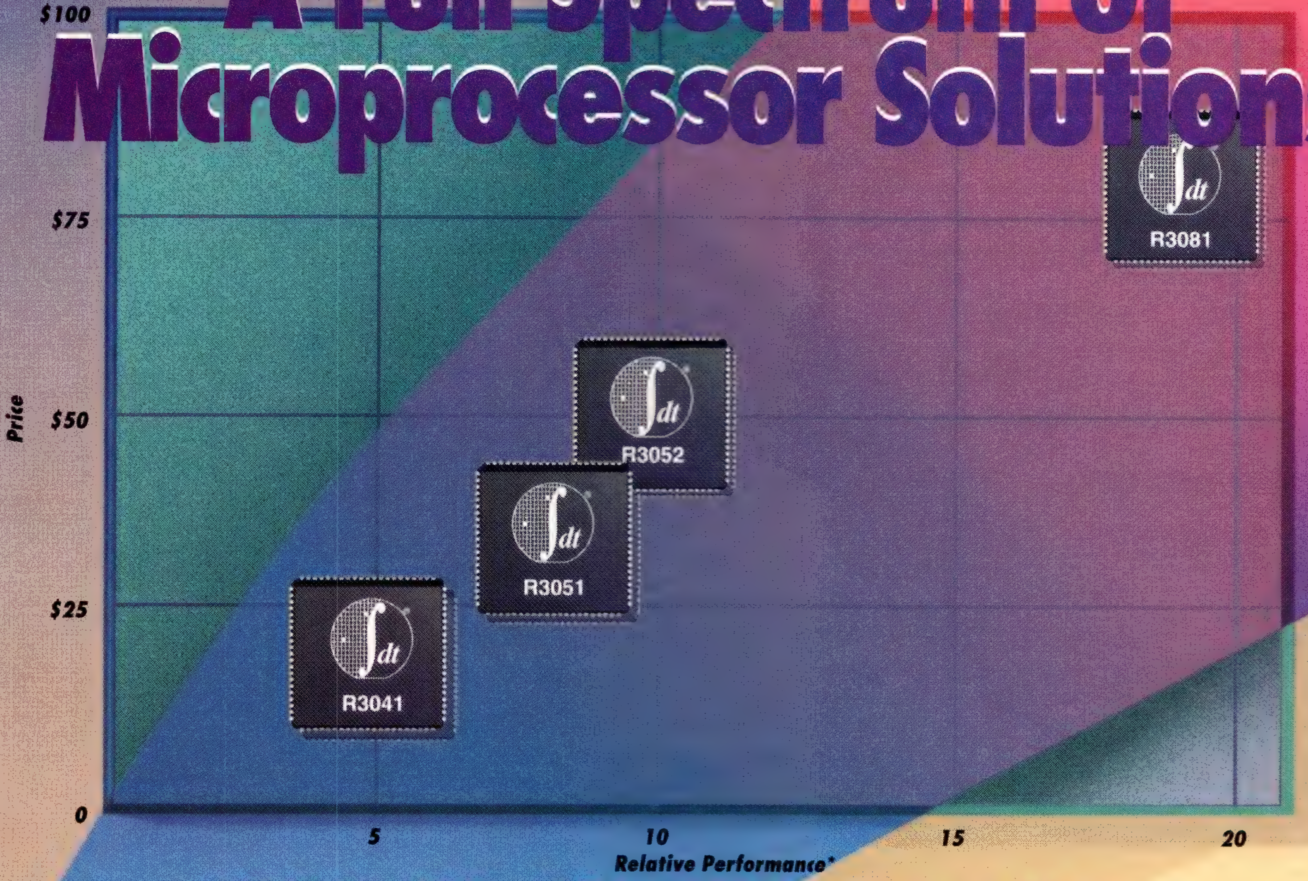

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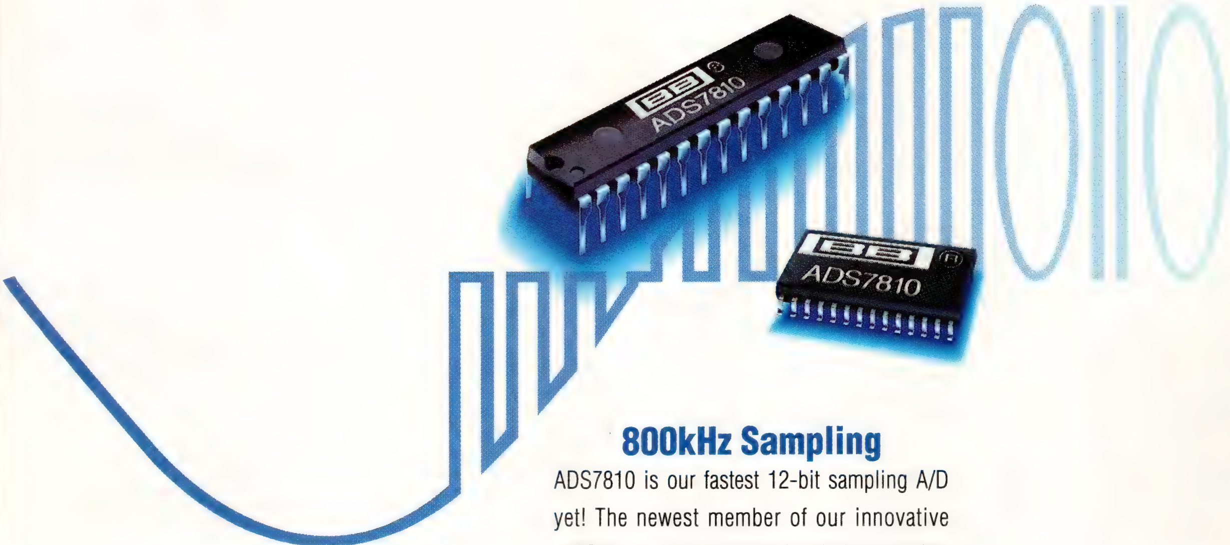

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CIRCLE 169 FOR U.S. RESPONSE **CIRCLE 170 FOR RESPONSE OUTSIDE THE U.S.**

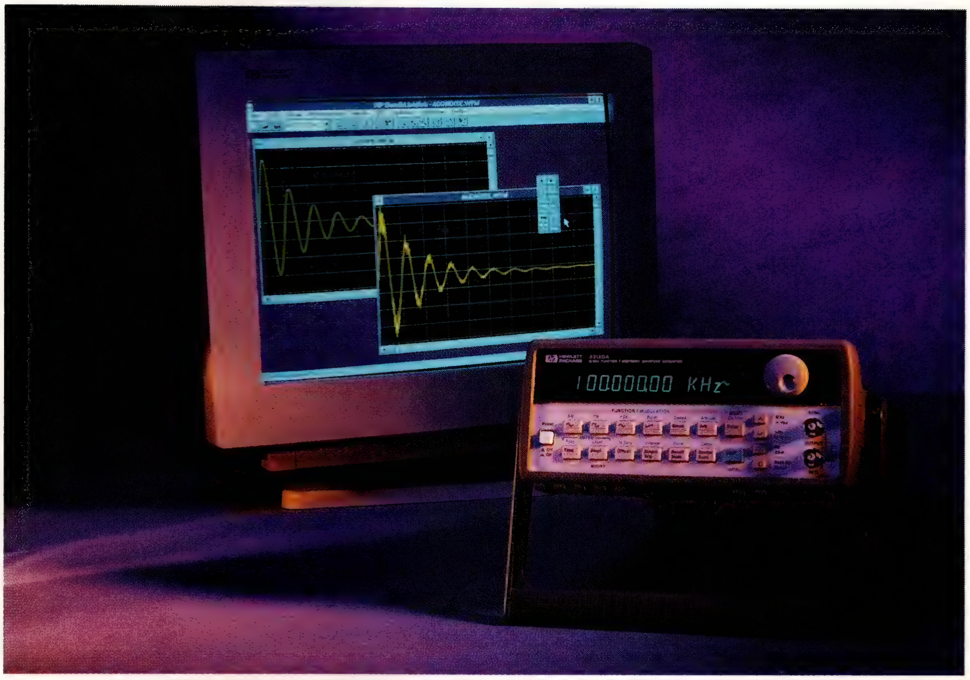
Function generators take on a digital tone

Synthesis techniques bring tremendous flexibility to an old benchtop standby.

BY JOHN NOVELLINO

An invasion of digital technology over the past few years has changed the face of function generation. Today's instruments offer much more capability and flexibility than those of even the recent past. However, what's also resulted is a certain amount of confusion over what a function generator actually is.

A number of traditional analog-based function generators containing RC circuits that tune the unit's output frequency are still available. And many of these generators are still bought every year. But most new products being introduced create their output signals digitally, primarily using direct digital synthesis (DDS). In a DDS-based function generator, the output function is stored in a waveform memory, whose contents are clocked out to a digital-to-analog converter *(see "How direct digital synthesis works," p. 93).*



One of the biggest advantages of DDS-based function generators is that manufacturers can relatively easily and inexpensively endow them with some arbitrary-waveform capability. Exactly how much arbitrary capability is a decision the instrument manufacturer must make based on the market niche it wants to target.

That leads to some fine distinctions being made, with some manufacturers offering products called function generators, arbitrary-function generators, and arbitrary-waveform generators. Generally, the units known as arbitrary-waveform generators are traditional, full-capability instruments (these aren't included in the product listing on p. 96).

All that's needed to turn a DDS-based function generator into an arbitrary-waveform or arbitrary-function generator is the addition of another memory in which users can load a custom waveform, says David Kruse, a sales and marketing engineer at Stanford Research Systems, Sunnyvale, Calif. The result is synthesized function generators with arbitrary capability priced as low as about $1000, he notes.

According to Kruse, "That's pretty much invading a lot of the territory that traditionally went to just function generators." As for the future, he says, "I think the distinction between function generator and arbitrary-waveform generator is going to become a question of marketing." A large part of the distinction will be how much memory and how many ease-of-use features the instruments will include. Both add cost and will become differentiating factors.

The ease with which arbitrary waveforms can be specified is especially important in full-capability arbitrary generators, if users are to get the maximum benefit out of these instruments. Entry and editing schemes may include downloading of stored real-world waveforms, mathematical specification, or various drawing methods. An arbitrary-function generator usually limits these techniques.

Another important difference between DDS-based function generators and full-capability arbitrary-waveform generators is the method used to change frequencies. In the latter, operators change the frequency by varying the clock rate, and thus the rate at which the stored points are clocked out of memory. In a DDS-based system, the frequency is changed by varying the number of points executed from the record memory, says Bruce Virell, signal sources marketing manager at Tektronix Inc., Beaverton, Ore.

Eliminating points is going to reduce waveform definition. As a result, generator designers must carefully choose the filter algorithms that will create the analog waveforms. This isn't a problem with sine waves because it's easy to build a filter that generates an accurate sine function, notes Virell. Functions with linear elements—including triangle and square waves—are affected more, because as points are eliminated, edges can start to move.

"Say you're creating a square wave and you've got a certain positive transition on the waveform that's associated with a given point in time. As you start scanning points in memory and start skipping points, that clock edge will move, and that's not very desirable," says Virell. "If you're trying to re-create a waveform, you'd like to have the data points remain consistent within that arbitrary memory. So that's a distinction to be made between these function generators and arbitrary-waveform generators."

Nevertheless, with technology improvements and cost reductions, the movement toward digital techniques will continue to its logical conclusion, according to David Madsen, product manager for instrumentation at Analogic Corp., Peabody, Mass. "If you're talking about several years from now, the older-type function generators will probably cease to exist," he says. "They will be replaced by pure arbitrary-waveform generators with built-in functions already preprogrammed to produce the sine and everything else that's done with analog techniques today."

The limiting factor at the moment is the price of the very fast DACs and the fast memory needed to accurately create the desired functions. To get a reasonable-quality 10-MHz sine wave with 20 points per period, explains Madsen, the generator would have to clock it out of memory at 200 MHz. "Now 200-MHz DACs aren't easy to find and they aren't that cheap," he says. "And the memory that supplies that DAC also has to be fast. That is not cheap, although it is getting cheaper."

As the costs of these components drop during the next few years, "it will actually be cheaper to produce an arbitrary-waveform generator with the same quality with which you could produce an analog-function generator," says Madsen. "And you still have the advantage of using it as an arbitrary-waveform generator."

The bottom line is a tremendous improvement in the price-performance ratio of function generators. "It really is kind of phenomenal that you now have full sweep capability, full modulation capabilities, full programmability, even the arbitrary waveforms," says Mark Bailey, a product marketing manager for Hewlett-Packard's Personal Measurement Operation in Loveland, Colo. "All of this is built-in for under $2000."

An interesting example of the changes wrought by digital synthesis is the frequency accuracy of the newer function generators, which Bailey says seem to be affecting sales of frequency counters. One of the major applications of counters used to be to measure the actual frequency coming out of a function generator. "Nowadays, with synthesized generation techniques, if you dial up 1.234567 MHz, it's going to be pretty darn close," says Bailey. It's like 10-ppm kind of accuracy."

> **The bottom line is a tremendous improvement in the price-performance ratio of function generators.**

Bailey believes this is part of a larger trend in test and measurement, with no end in sight. "I don't see anything to necessarily halt the trend of more power for less money," he says. "People expect that if they're going to pay the same amount of money they're going to get more power. Or for the same kind of capability, they're probably going to pay less for the next generation."

When selecting a function generator, users should consider several features that may be important to their application. Not all units will allow them to vary the phase of the output signal. This capability permits delayed outputs. In addition, not all generators include sync pulses that make it possible for users to synchronize their outputs with other instruments. Depending on the application, another useful feature is a voltage-controlled-oscillator (VCO) input, which allows external frequency modulation of the generator's output signal.

One key specification is the sine wave's total harmonic distortion (THD). Analogic's Madsen notes that for digital instruments, THD is often specified at a frequency well below the instrument's maximum output frequency. If the purity of the output signal is important, he notes, users should make sure the specifications are suitable within the frequency range of interest.

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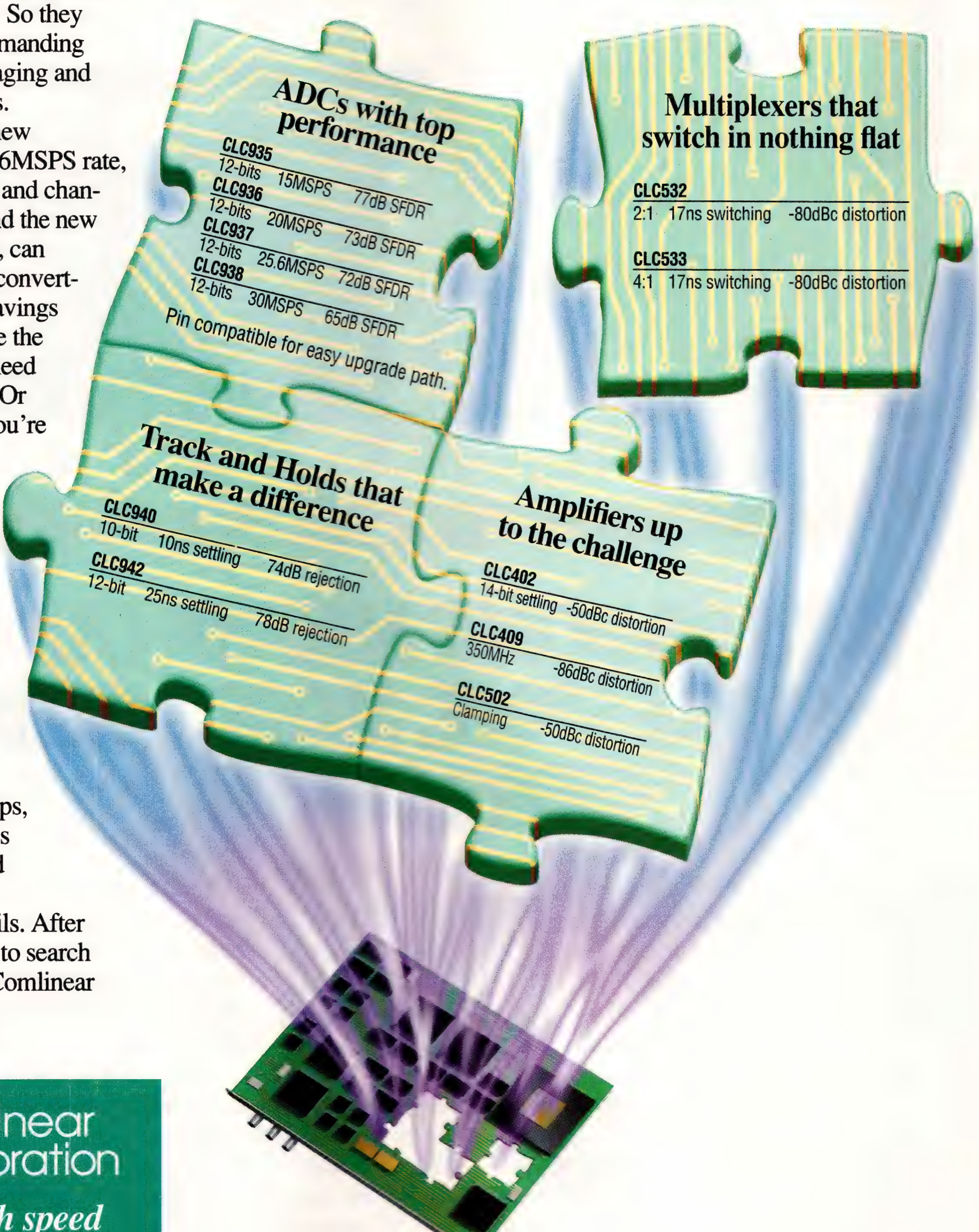

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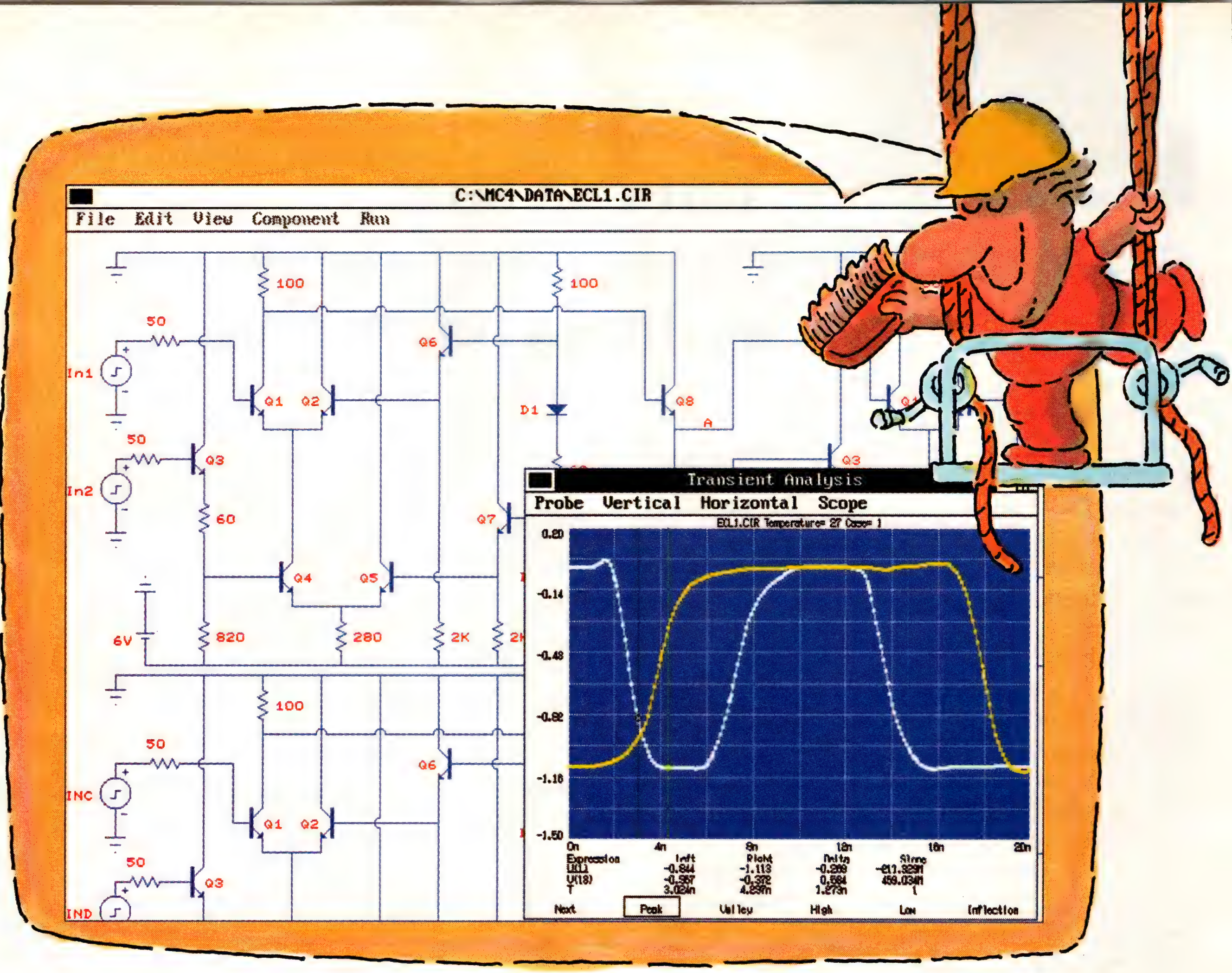

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Expression      Left      Right     Delta     Slope
V(1)           -0.844    -1.113    -0.269   -211.329M
V(18)          -0.567    -0.372     0.584    459.034M
T               3.024n    4.297n    1.273n    1
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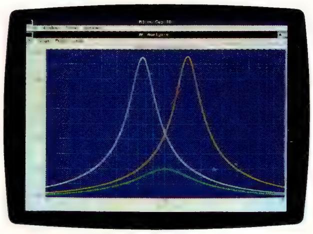
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Function generators test digital devices

Digitally based function generators give engineers expanded test capabilities.

BY DOUGLAS BARKER

Fluke Corp., Box 9090, Everett, WA 98206; (206) 347-6100.

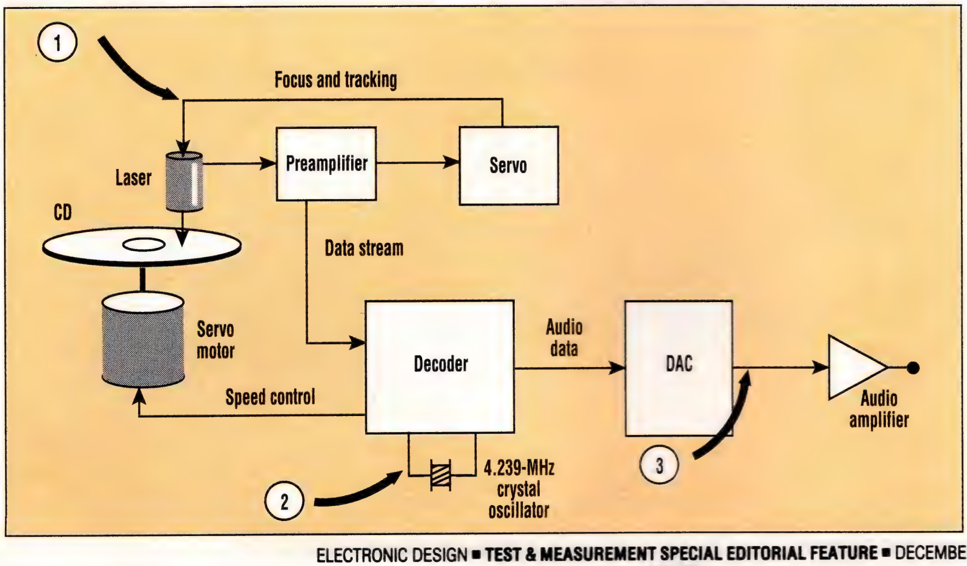
Function generators are very helpful in many traditional applications where a simple continuous-wave test signal is needed. When troubleshooting an analog signal path, the trusty benchtop function generator with its sine, square, and triangle waveforms becomes an ideal signal source. But test requirements are getting increasingly complex, often including both digital and analog signals and with more critical voltage and frequency parameters. To keep pace, much more capability is built into the newer function generators, giving users a number of advantages.

One particularly important technology now used in function generators is direct digital synthesis (DDS), which is replacing traditional analog signal-generation methods. These new types of function generators are very useful for testing devices like compact-disc players, which incorporate a mix of analog and digital technology.

A CD player contains a complex control system that employs focus and tracking servo motors on the laser and another servo motor that rotates the disc at different speeds, depending on the particular track. The players have a tendency to "skip," meaning the control system loses lock when subjected to physical shock, such as when driving over a rough road.

Designers need to characterize the reaction and recovery time of the control system for such a disturbance. This can be done by injecting simulated pulses directly into the control system just before the laser *(Fig. 1)*. The system's recovery time is then measured with a digital storage oscilloscope (DSO).

The first step is to choose a pulse from the function generator's menu of outputs that best resembles an actual disturbance. A DDS-based function generator offers the advantage of a larger library of standard waveforms because the waveforms are stored digitally and loaded into waveform memory as needed *(see "How Direct Digital Synthesis Works," p. 93)*. For example, the PM 5139 provides a choice of sine, triangular, square, and sine^2 pulses as well as continuous waveforms. To test the CD player, the sine^2 pulse most accurately simulates the error voltage that results from a mechanical shock in the control system.

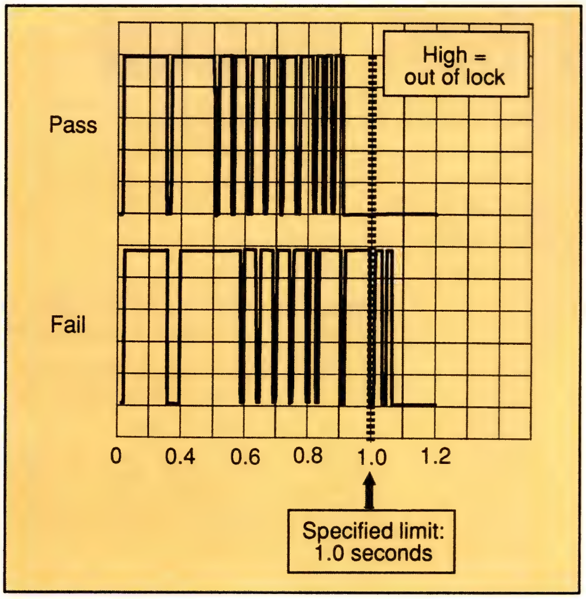


1. This block diagram of a CD player indicates where to inject signals to evaluate the system's recovery from mechanical shock (1), to substitute for the clock (2), or to characterize the audio amplifier (3).

If the instrument's standard library doesn't offer a usable waveform, the user can create a custom waveform using the arbitrary waveform capability offered in most DDS-based function generators. However, the arb capability is usually somewhat limited in instruments commonly labeled "arbitrary/function generators," compared with a full-capability arbitrary waveform generator. Users shopping for an instrument with dual capability should closely inspect the amount of control available over sample rate, memory depth, and the number of bits of vertical resolution—traditional arbitrary waveform generator specifications. Quite often, the instrument's sample rate or the memory depth is fixed.

True arbitrary waveform generators offer better control over these parameters but, conversely, lack common function generator features (real-time analog modulation capability) and easy, intuitive setting of parameters (frequency and amplitude). As a result, the choice of instrument will result in a trade off of arbitrary- and function-generator capability.

The precise pulse characteristics must still be determined. Immunity to shock and vibration, which is critically important in a CD player, can be



2. After forcing the CD player to an out-of-lock condition, a digital scope can be used to measure the seek time, which is how long the system takes to reestablish lock.

looked at in several ways. One way is to vary the disturbance pulse's amplitude and pulse width to get a threshold level of immunity to one pulse. From experience, a base-line value can be established to separate "good" and "bad" performance.

After deciding on a suitable disturbance pulse, the user must set up the function generator to produce one complete cycle of the pulse. This is accomplished with the burst mode. The number of cycles in the burst is selectable by the user, triggered either as a single-shot or programmed for a regular repetition rate with the internal trigger generator. By setting the number of cycles to 1 and the trigger source to "single," the burst function can be configured to send out a single-shot pulse for each press of a front-panel trigger button.

For the example CD tests, the pulse frequency was set to 150 Hz to get a pulse width of about 3 ms, which best matched actual disturbance pulses seen in the control loop. The amplitude was set to deliver enough voltage to make the CD player skip (approximately 1 V p-p).

Another way to evaluate immunity to shock is by looking at the control system's ability to withstand multiple "hits" without losing lock. The burst mode can be used to create a string of multiple pulses that simulate mechanical ringing, which often occurs when a complex mechanism is subjected to physical shock.

For this test, the user sets the pulse amplitude and frequency to known-good levels (ones that won't cause a single-shot problem). The number of pulses is then increased until a problem occurs or the player is determined to be immune to multiple shocks.

Newer function generators can create counted burst functions well into the thousands of cycles. In the example CD player, the control system's recovery time was fast enough that injecting multiple 3-ms pulses caused no problems.

If the CD player does "skip," either because of mechanical shock or a scratched or dirty compact disc, the control system must react to reestablish lock. If the disturbance is too severe, the player will stop altogether. A number of adjustments in a typical CD player, including loop gain and balance, affect the control system's ability to reestablish a particular track. Thus, a good measure of that performance is the "seek time" required.

Distinguishing a good seek time from a bad one is a matter of customer expectations and the fundamental design characteristics of the control system. In the manufacturing environment, the selected specification must be easy to obtain when adjustment procedures are properly followed. If the seek time gets too long, the loop parameters probably need to be "tweaked" again.

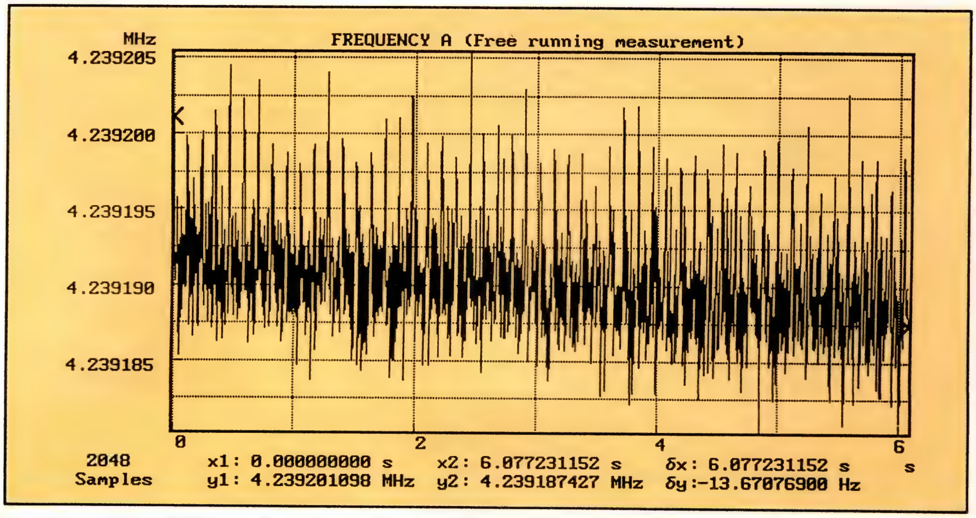
The control system sends an "out-of-lock" signal to the microprocessor while it reestablishes lock. The easiest way to measure the seek time is to record this signal on a DSO in single-shot mode. The armed scope waits for the out-of-lock signal to occur.

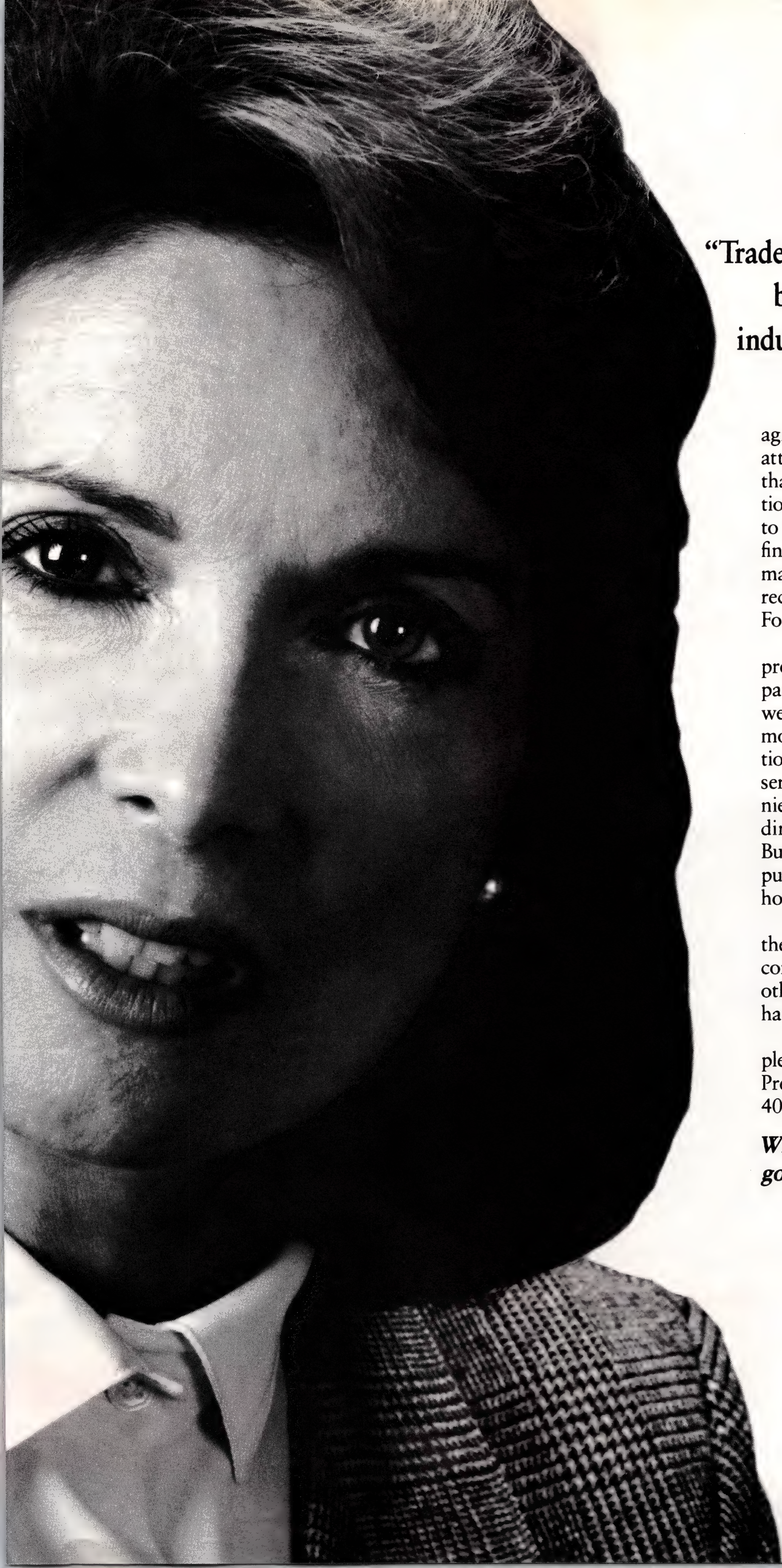
Then the operator uses the cursors to determine the seek time. In the example CD, 1.0 seconds was the specified limit for an acceptable unit. A Fluke PM 3394 CombiScope with a time base set to 200 ms/div. was used to take the data *(Fig. 2)*.

Designers can also evaluate several parameters of a CD player's oscillator by disabling or removing the oscillator and injecting a signal from a function generator. More often than not, these oscillators are crystal oscillators, with the crystal and oscillator sealed in the same package as a discrete component. A typical personal computer may have a dozen such oscillators.

Function generators are often used as substitutes for oscillators. DDS-based instruments, which deliver the frequency resolution needed to precisely dial

3. The CD player's measured clock jitter (recorded on a digital oscilloscope) had a modulation frequency of about 10 Hz and a frequency variation of about 30 Hz.





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in the odd frequencies, possess the stability and accuracy of an internal crystal reference oscillator. An added advantage of DDS technology is that frequencies can be changed almost instantaneously and with no phase discontinuity, a feature especially helpful during the "re-trace" of frequency sweeps or in simulating a frequency-shift-keyed signal.

A sine wave is generally the best choice for oscillator substitution because of the narrowband signal energy around the carrier frequency. Square waves, on the other hand, have sharp edges rich in harmonic content, which may cause nonlinearity problems in the oscillator. In the example CD player, the function generator injects a 4.239-MHz sine wave in place of the oscillator *(Fig. 1, again)*.

Oscillator sensitivity can then be checked by determining the minimum drive level needed to operate the oscillator. This test is made easier by the fact that most newer DDS-based function generators are remotely programmable, which means the output amplitude controls are also programmable. The output vernier is replaced by fixed attenuators with much higher accuracy and resolution.

Despite this additional precision, the exact drive level seen at the load depends entirely on its impedance. Note that the amplitude setting in some generators assumes an open (high-impedance) circuit and in others it assumes a 50-Ω load. Either way, the final check is always done with the trusty oscilloscope probing at the device under test to determine the actual level.

Newer function generators can create counted burst functions well into the thousands of cycles.

With the function generator in sine-wave mode, the CD-player oscillator circuit needed a drive level of only 0.8 V p-p. With the crystal reinstalled, the signal level was well over 3 V p-p, so the player has plenty of margin in the oscillator for gain.

The CD player's tolerance to frequency drift can also be evaluated easily by varying the generator's front-panel carrier frequency, again with no phase discontinuity during each frequency change. The player that was tested tolerated reference frequencies from 4.3 to 10.7 MHz with continued reliable operation. Such a wide frequency range means that the design has no marginal timing problems to worry about.

Even the least expensive crystal oscillator can deliver accuracies exceeding 0.05%. The device used in the CD player is a

HOW DIRECT DIGITAL SYNTHESIS WORKS

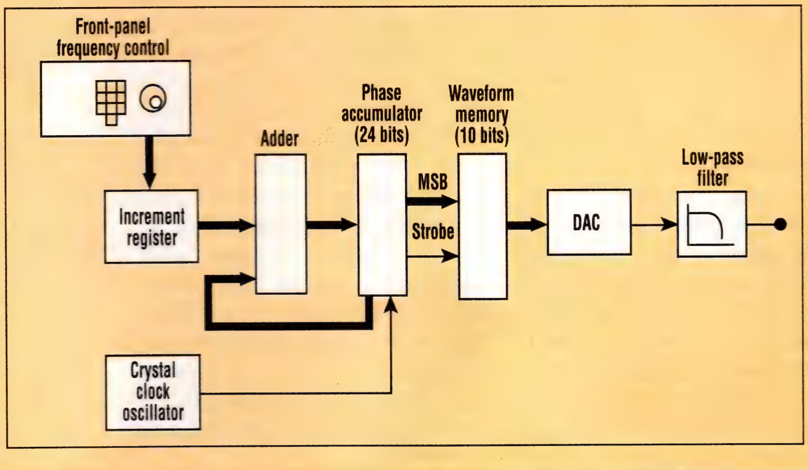
Direct digital synthesis is a natural fit for the new generation of function generators, which are starting to replace both analog instruments and conventional synthesizers. DDS has two main advantages over its analog predecessors: extremely fine resolution and the stability of a crystal reference oscillator. And unlike synthesizers based on phase-locked loops, DDS instruments can change frequency almost instantaneously and with no frequency discontinuity.

Furthermore, because waveforms are stored digitally, creating a large library of waveforms is relatively easy in the DDS-based instrument. The waveform memory can be loaded with standard functions stored in ROM, or arbitrary waveforms can be loaded through an interface bus.

The heart of a DDS system is the phase accumulator, which is nothing more than a long register that keeps track of the relative phase of the signal *(see the diagram)*. The output frequency is set by controlling the value in the phase-increment register.

Each phase increment is added to the value in the phase accumulator at a rate set by the instrument's crystal clock oscillator. The phase-increment register determines how many clock cycles are needed to step through the signal's entire phase, which in turn determines the output frequency. The larger the increment value, the higher the output frequency.

The number of bits in the phase accumulator determines the instrument's frequency resolution. For example, a 24-bit phase accumulator provides 10-Hz resolution at 20 MHz (7 digits). The most significant bits of the accumulator form the address that's strobed out to the waveform memory. A 32-kbyte waveform memory depth corresponds to a 15-bit-wide address bus. The contents of the waveform memory are clocked out to the digital-to-analog converter to generate the waveform. An analog low-pass filter may be switched in to suppress sample-rate noise present at the output.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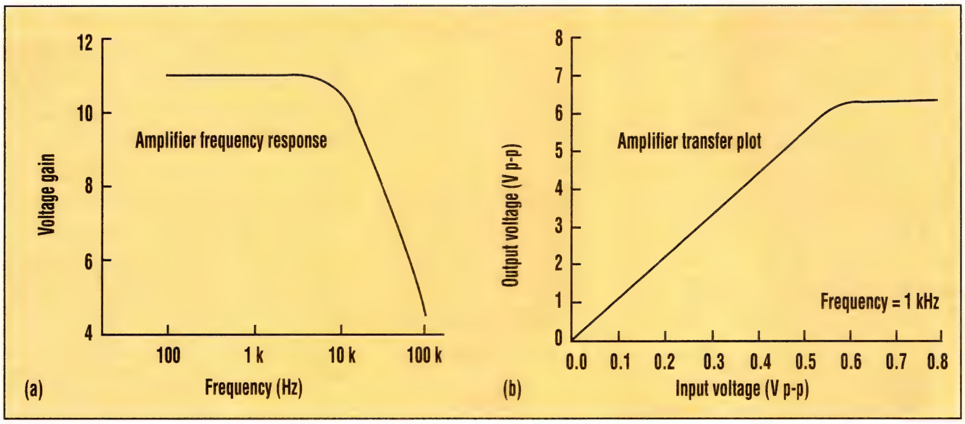

4. The conventional amplifier frequency response (a) and voltage transfer plots (b) are ideal applications for DDS-based function generators. That's because the instruments can be quickly programmed to create frequency- or amplitude-swept input signals.

simple AT strip resonator with 0.05% frequency accuracy, which is adequate for the application. For improved stability over temperature, more elaborate (and expensive) oscillators are available.

Clock jitter can also cause failures in digital systems that depend on complex timing relationships synchronized to the clock. Because the entire CD player system is referenced to the oscillator, any uncertainty in timing relationships that show up as jitter will degrade the music quality.

A noticeable amount of jitter was present in the oscillator signal when it was examined with the CombiScope in analog mode. This timing jitter was verified after some investigation with a PM 6680 frequency counter that measured the clock frequency at 600 readings/s. The jitter turned out to be periodic with a modulation frequency of approximately 10 Hz as well as a 30-Hz frequency deviation *(Fig. 3)*. The source of the jitter was found to be the main disk motor, which modulated the oscillator through the power-supply line.

Jitter can be simulated by function generators using frequency modulation. By setting the internal modulation frequency to 10 Hz in FM mode and varying the deviation level, the relative sensitivity of the CD player to clock jitter can be evaluated. The PM 5139 can generate frequency modulation as low as 0.01%, which corresponds to 880-Hz p-p at the oscillator's carrier frequency.

To evaluate the upper margin that could be withstood by the system, the deviation was increased until the CD player stopped working. The unit handled a 10-kHz deviation without a noticeable failure.

The more subtle effect of clock jitter on reproduced sound quality at lower deviation levels is also an important concern. But it can be evaluated only with more specialized audio-distortion analyzers.

The key analog component in the otherwise digital CD player is the audio amplifier, which supplies line-level audio to drive a preamplifier or a pair of headphones. Although audio-amplifier testing has changed little over the years, function generators have new capabilities that make the process somewhat easier.

For instance, amplifier testing is an excellent candidate for automation because the task requires gathering data over multiple frequencies and amplitude levels. And because the amplitude vernier controls were replaced with a programmable attenuator on DDS-based function generators, voltage levels can be set faster and more accurately over the bus. In addition, frequency can be set over the bus with many digits of resolution and with stability typically in the 10 ppm range over time and temperature.

The ready availability of instrument-oriented programming environments, such as National Instruments LabWindows, and an existing library of instrument drivers makes the process of programming instruments easy enough to be done on an ad hoc project level. Graphical-user-interface libraries provided with LabWindows allow collected data to be plotted quickly.

The type of bus interface a function generator should be equipped with depends on the application. The IEEE-488 bus, or GPIB, is best for applications involving multiple instruments under simultaneous control from one controller. It's also suitable when lots of data must be transferred, like uploading a waveform from a scope to a PC. Addressing concerns are also handled on the bus level.

RS-232, on the other hand, is much less expensive because every personal computer has one or two COM ports, and a function generator requires relatively little bus traffic to control. Fortunately, function-generator vendors now commonly offer both GPIB and RS-232 interfaces in the same instrument so the user can get the best of both worlds.

To test the CD player's amplifier, the function generator was connected to the amplifier's input. An oscilloscope or a digital multimeter (DMM) can record both the input and output peak-to-peak voltages needed to calculate the standard transfer functions.

Newer generators offer a sweep mode that can test the amplifier's frequency response. These units can be programmed in a data-collection loop that changes the generator frequency while a scope or DMM measures the input and output voltages *(Fig. 4a)*. Similarly, an amplitude sweep can be programmed to create an amplitude transfer plot at a fixed frequency *(Fig. 4b)*.

The example amplifier was

tested in-circuit and the frequency roll-off was largely governed by the CD player's antialias filter, which is a simple analog RC network that rejects the 44-kHz sample noise. Higher-end CD players employing oversampling techniques will have audio amplifiers with frequency responses extending well above 100 kHz.

Directly connecting a function generator to the input of an audio amplifier will likely affect the amplifier's bias point. That's because function generators have dc-coupled outputs in order to ensure good low-frequency flatness. In fact, DDS-based function generators extend low-end coverage well into the microhertz range.

For the tests on the example CD player, this problem was solved by using the function generator's dc offset to match the dc bias point of the amplifier. The point was measured as 6.8 V by a digital multimeter. The dc bias levels in newer function generators are programmable and can be set by a separate digital-to-analog converter that typically provides 100-mV resolution. Matching bias levels is acceptable for low-voltage applications, such as this one.

However, users must be careful not to back-bias a function generator. Although most function generators incorporate protective relays or "crowbar" diodes in the output, their ability to provide absolute protection is limited. Needless to say, a damaged output amplifier is one of the most common reasons a function generator is returned for service.

Unfortunately, ac coupling is often necessary for higher-voltage applications or sensitive circuitry that objects to the low-impedance load. Although ac coupling has the disadvantage of low-frequency roll-off, a blocking capacitor between the generator and amplifier will work if the user is interested only in the amplifier's high-frequency roll-off in the 20-kHz to 100-kHz range.

Douglas Barker, product marketing manager with the Fluke Corp., received a BSEE and MSEE from the University of Michigan, Ann Arbor, and an MBA from the University of Washington, Seattle. Before joining Fluke, Barker was a manufacturing development engineer with the Hewlett-Packard Co.

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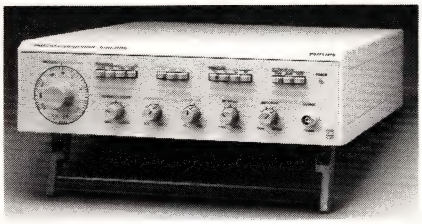
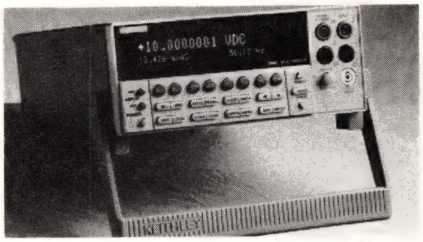


The 2-MHz PM 5135 function generator possesses a versatile sweep function with a logarithmic characteristic and a continuously variable sweep ratio of from 1 to 2000. Users can select single or continuous sweeps. Sweep range is 3.5 decades, and the sweep period is continuously adjustable from 10 to 150 seconds. Users can manually trigger the sweep with a pushbutton or use an external source. Attenuation includes a 0-to-60-dB range in 10-dB increments, and a 0-to-20-dB continuous adjustment. Sine, triangle, and square waves are pushbutton selected, and duty cycle is a standard 50%. A ±10-V dc offset is available. The offset can also be produced without an ac component. The PM 5135 costs $795, with delivery in four weeks.

Fluke Corp.
P.O. Box 9090
Everett, WA 98206-9090
(206) 347-6100
▶ CIRCLE 503



▼ 8.5-DIGIT DMM OFFERS WIDE DYNAMIC RANGE

The Model 2002 digital multimeter delivers 8.5-digit resolution without extensive averaging or filtering. The result is a faster response to small input changes and a broad dynamic range so users can measure from 0.1 μV to 20 V on one range, minimizing range-shift errors. The unit's ac voltage bandwidth is 1 Hz to 2 MHz, and an ac crest factor capability warns if the signal's crest factor (the peak-to-rms ratio) is affecting specified accuracy. Frequency measurements to 15 MHz can be made with an adjustable trigger. The meter can take 44 readings per second at full accuracy, and more than 2000 readings per second at 4.5-digit resolution. A back-panel option slot accepts one of a number of application-specific modules. One option is a 1-pV, 100-pΩ preamp. Also, two multiplexer cards eliminate the need for a separate scanner. The Model 2002 costs $4995, with delivery within six weeks.

Keithley Instruments Inc.
28775 Aurora Rd.
Cleveland, OH 44139
(800) 552-1115
(216) 248-0400
▶ CIRCLE 504

FUNCTION GENERATORS

Manufacturer	Model/ Price	Frequency range	Type of functions (waveforms)	Type of internal sweep	Type of internal modulation	Max. output (V p-p into 50 ohms)	Remarks
Analogic Corp. 8 Centennial Dr. Centennial Industrial Park Peabody, MA 01961 (508) 977-3000	2310/ $695	10 mHz - 10-MHz	Sine, triangle, square, dc	—	—	10	VCO input; variable symmetry.
	2311/ $995	10 mHz - 10 MHz	Sine, triangle, square, dc	Linear	AM, FM	10	Variable symmetry; external sweep; external AM.
	2410/ $1695	4 mHz - 10 MHz	Sine, triangle, square, dc	—	—	10	External VCO, AM; programmable variable symmetry; separate offset generator.
	2411/ $1995	4 mHz - 10 MHz	Sine, triangle, square, dc, pulse	Linear, logarithmic	AM, FM	10	Same as 2410, plus burst mode.
	2605/ $1995	To 4 MHz sine, 5 MHz square, 100 kHz triangle	Sine, triangle, square, ramp, noise, arbitrary	(User programmable)	AM, FM	10	0.01 sample/s to 10 Msample/s arbitrary capability.
	2420/ $2795	20 mHz - 20 MHz	Sine, triangle, square, pulse, dc	—	—	15	Same as 2410, plus burst mode and variable phase.
	2620/ $3495	To 10 MHz sine and square, 1 MHz triangle	Sine, triangle, square, ramp, noise, arbitrary	(User programmable)	AM, FM	10	0.01 sample/s to 25 Msample/s arbitrary capability.
American Reliance Inc. 9952 E. Baldwin Pl. El Monte, CA 91731 (800) 654-9838 (818) 303-6688	FG-506/ $575	2 Hz - 6 MHz	Sine, triangle, square, dc	Linear, logarithmic	AM, FM, duty-cycle	10	Includes 6-1/2-digit, 100-MHz frequency counter.
	FG-513/ $875	2 Hz - 13 MHz	Sine, triangle, square, dc	Linear, logarithmic	AM, FM, duty-cycle	10	Includes 6-1/2-digit, 100-MHz frequency counter.
B&K-Precision Div. Maxtec International Corp. 6470 W. Cortland St. Chicago, IL 60635 (312) 889-1448	3001/ $79	20 Hz - 150 kHz	Sine, square	—	—	1.2 V rms (no load)	Hand-held; battery powered.
	3011/ $269	0.2 Hz - 2 MHz	Sine, triangle, square, pulse, TTL, CMOS	—	—	10	External sweep, FM; built-in 4-digit counter.
	2005A/ $275	100 kHz - 450 MHz	Sine	—	AM	100 mV rms	—

We improved our line of voltage references by making one tiny adjustment.

	LM4040	LM4431	LM9140	LM4041
Initial Voltage Tolerance (%)	±0.1, ±0.2, ±0.5, ±1.0, ±2.0	±2.0	±0.5	±0.1, ±0.2, ±0.5, ±1.0, ±2.0
Voltage Options (V)	2.5, 4.096, 5.0, 8.192, 10.0	2.5	2.5, 4.096, 5.0, 10.0	Adjustable, 1.2
Tempco (max)	100ppm/°C, 150ppm/°C	30ppm/°C (typ)	25ppm/°C	100ppm/°C, 150ppm/°C
Packages	SOT-23, SO-8, TO-92	SOT-23	TO-92	SOT-23, SO-8, TO-92
Temp range	-40°C to +85°C	0°C to +70°C	-40°C to +85°C	-40°C to +85°C
Price (100 pc)	$0.79	$0.69	$1.75	$0.79

Here's the big difference: Our new LM4041 is the only adjustable voltage reference in a subminiature SOT-23 package. So it's the only reference that combines the smallest footprint with the flexibility to adjust for a wide range of voltages (1.24V to 10V). The LM4041 is the latest upgrade to our line of high-performance, easy-to-use voltage references—a family that now includes both general-purpose devices as well as high-precision references like our new LM9140. And they're all available in a wide variety of voltage ranges and packages. To find out more, call us at **1-800-NAT-SEMI (628-7364) Ext. 245**. We'll send you free samples, along with datasheets and a complete reference family selection guide. That's the big deal.

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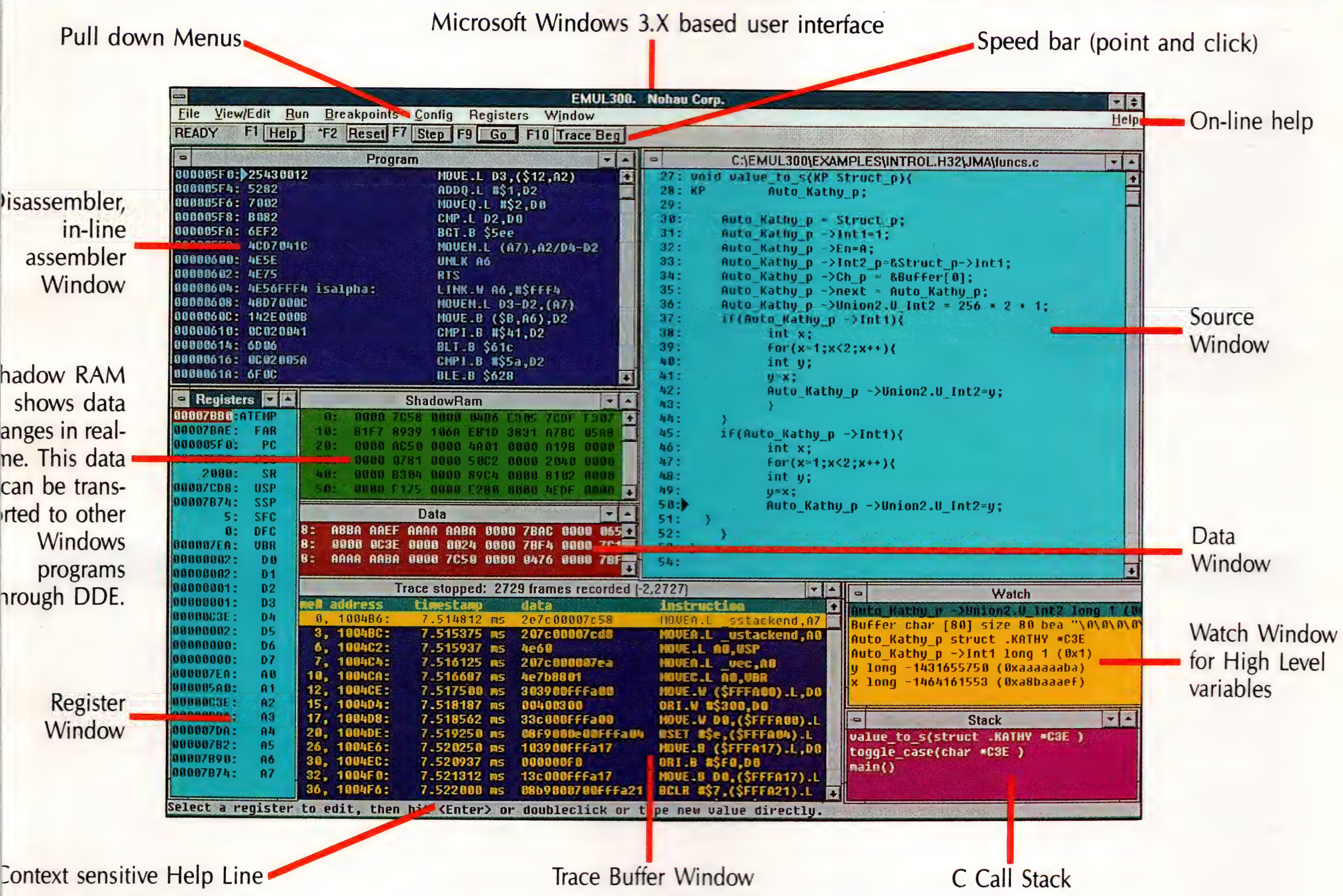
(Tel: 1-800-628-7364, Ext. 245; Fax: 1-800-888-5113)

FUNCTION GENERATORS

Manufacturer	Model/ Price	Frequency range	Type of functions (waveforms)	Type of internal sweep	Type of internal modulation	Max. output (V p-p into 50 ohms)	Remarks
B&K-Precision Div. Maxtec International Corp. 6470 W. Cortland St. Chicago, IL 60635 (312) 889-1448	3017A/ $339	0.2 Hz - 2 MHz	Sine, triangle, square, pulse, TTL, CMOS	Linear, logarithmic	—	10	External FM; adjustable sweep start/stop.
	3022/ $479	0.2 Hz - 2 MHz	Sine, triangle, square, pulse, TTL, CMOS, tone burst	Linear, logarithmic	AM, FM	10	Built-in 5-digit counter.
	3026/ $629	0.5 Hz - 5 MHz	Sine, triangle, square, pulse, TTL, CMOS	Linear, logarithmic	AM, FM	10	Built-in 5-digit counter.
	3030/ $865	1 MHz - 5 MHz	Sine, triangle, square, ramp, pulse, tone burst	Linear, logarithmic	—	10	External FM; adjustable sweep start/stop.
	3040/ $1195	0.1 Hz - 13 MHz	Sine, triangle, square, pulse, TTL, tone burst	Linear	AM, FM	10	Built-in 6-digit counter.
Fluke Corp. P.O. Box 9090 Everett, WA 98206 (800) 443-5853 (206) 347-6100	PM 5135/ $795	1 mHz - 2 MHz	Sine, triangle, square	Linear	—	10	Analog instrument.
	PM 5138/ $3700	0.1 MHz - 10 MHz	Sine, triangle, square, ramp, pulse, arbitrary	Linear, logarithmic	AM, FM, PSK, gate, burst	10	Direct digital synthesis; IEEE-488 option, $450.
	PM 5139/ $4300	0.1 mHz - 20 MHz	Sine, triangle, square, ramp, pulse (sine, triangle, square, sine^2), arbitrary	Linear, logarithmic	AM, FM, PSK, gate, burst	10	Direct digital synthesis; IEEE-488 option, $450.
	PM 5193/ $4925	0.1 mHz - 50 MHz	Sine, triangle, square, ramp, sine^2, pulse	Linear, logarithmic	AM, FM, gate, burst	10	IEEE-488 standard; rack mount standard.
Global Specialties 70 Fulton Ter. New Haven, CT 06512 (203) 466-6103	2001/ $178.50	1 Hz - 100 kHz	Sine, triangle, square, TTL	—	—	10 V (open)	External sweep, variable dc offset.
	2002/$219.95	0.2 Hz - 2 MHz	Sine, triangle, square, TTL	—	—	10	External sweep; duty-cycle, symmetry controls.
	2006/ $279.95	0.2 Hz - 2 MHz	Sine, triangle, square, TTL	Linear	—	10	Variable dc offset; duty-cycle control.
	2003/ $499.95	0 - 1.6 MHz	Sine, triangle, square, TTL	Linear	—	10	Trigger, burst, hop, gate modes, RS-485 opt.
Hameg Instruments Inc. 1939 Plaza Real Oceanside, CA 92056 (619) 630-4080	HM8030-4/ $576*	0.3 Hz - 3 MHz	Sine, triangle, square, TTL	Linar	—	10	*Price includes HM8001 mainframe; external FM; variable dc offset.
	HM8130/ $1280	10 mHz - 10 MHz	Sine, triangle, square, ramp, pulse, arbitrary, TTL	Linear	—	10	External AM; RS-232, IEEE-488 opt.
Hewlett-Packard Co. Direct Marketing. Org. P.O. Box 58059 MS51L-SJ Santa Clara, CA 95051-8059 (800) 452-4844	33120A/ $1695	100 μHz - 15 MHz	Sine, triangle, square, ramp, exp. rise, exp. fall, (Sin X)/X	Linear, logarithmic	AM, FM, FSK, burst	10	Includes 12-bit, 40-Msample/s, 16-kpoint arbitrary capability; RS-232, IEEE-488 std.
	8904A/ $2600	0 - 600 kHz	Sine, triangle, square, ramp	—	AM, FM, PM	10	Limited arbitrary capability; multiple output opt.
	8111A/ $2700	1 Hz - 20 MHz	Sine, triangle, square ramp, pulse haver functions	—	—	16	Variable pulse width, duty cycle; trigger, gate modes; VCO input.
	3325B/ $4800	1 μHz - 21 MHz	Sine, triangle, square, ramp, pulse	Linear, logarithmic	AM, PM	10	RS-232, IEEE-488 std.

In-Circuit Emulators and Background Debuggers

68300 68HC16



```
000005F0:▶25430012                  MOVE.L D3,($12,A2)
000005F4: 5282                      ADDQ.L #$1,D2
000005F6: 7002                      MOVEQ.L #$2,D0
000005F8: B082                      CMP.L D2,D0
000005FA: 6EF2                      BGT.B $5ee
          4CD7041C                  MOVEM.L (A7),A2/D4-D2
00000600: 4E5E                      UNLK A6
00000602: 4E75                      RTS
00000604: 4E56FFF4 isalpha:         LINK.W A6,#$FFF4
00000608: 48D7000C                  MOVEM.L D3-D2,(A7)
0000060C: 142E000B                  MOVE.B ($B,A6),D2
00000610: 0C020041                  CMPI.B #$41,D2
00000614: 6D06                      BLT.B $61c
00000616: 0C02005A                  CMPI.B #$5a,D2
0000061A: 6F0C                      BLE.B $628
```

C:\EMUL300\EXAMPLES\INTROL.H32\JMA\funcs.c

```
void value_to_s(KP Struct_p){
KP          Auto_Kathy_p;

    Auto_Kathy_p = Struct_p;
    Auto_Kathy_p ->Int1=1;
    Auto_Kathy_p ->En=A;
    Auto_Kathy_p ->Int2_p=&Struct_p->Int1;
    Auto_Kathy_p ->Ch_p = &Buffer[0];
    Auto_Kathy_p ->next = Auto_Kathy_p;
    Auto_Kathy_p ->Union2.U_Int2 = 256 * 2 + 1;
    if(Auto_Kathy_p ->Int1){
        int x;
        for(x=1;x<2;x++){
        int y;
        y=x;
        Auto_Kathy_p ->Union2.U_Int2=y;
        }
    }
    if(Auto_Kathy_p ->Int1){
        int x;
        for(x=1;x<2;x++){
        int y;
        y=x;
        Auto_Kathy_p ->Union2.U_Int2=y;
  }
    }
```

```
00007BB6:ATEMP
00007BAE:  FAR
000005F0:   PC

    2000:   SR
00007CD8:  USP
00007B74:  SSP
       5:  SFC
       0:  DFC
000007EA:  VBR
00000002:   D0
00000002:   D1
00000001:   D2
00000001:   D3
00000C3E:   D4
00000002:   D5
00000000:   D6
00000000:   D7
000007EA:   A0
000005A0:   A1
00000C3E:   A2
          : A3
000007DA:   A4
000007B2:   A5
00007B90:   A6
00007B74:   A7
```

```
 0:  0000 7C58 0000 0406 E305 7CDF F307
10:  81F7 8939 106A EB1D 3831 A7BC 05A8
20:  0000 AC50 0000 4A01 0000 A19B 0000
     0000 0781 0000 50C2 0000 2040 0000
40:  0000 B304 0000 89C4 0000 8102 0000
50:  0000 F175 0000 E28A 0000 4EDF A0A0
```

```
8:  ABBA AAEF AAAA AABA 0000 7BAC 0000 065
8:  0000 0C3E 0000 0024 0000 7BF4 0000
8:  AAAA AABA 0000 7C58 0000 0476 0000 7BF
```

Trace stopped: 2729 frames recorded (-2,2727)

```
me# address   timestamp     data                  instruction
 0, 1004B6:   7.514812 ms   2e7c00007c58          MOVEA.L  sstackend,A7
 3, 1004BC:   7.515375 ms   207c00007cd8          MOVEA.L _ustackend,A0
 6, 1004C2:   7.515937 ms   4e60                  MOVE.L A0,USP
 7, 1004C4:   7.516125 ms   207c000007ea          MOVEA.L _vec,A0
10, 1004CA:   7.516687 ms   4e7b0801              MOVEC.L A0,VBR
12, 1004CE:   7.517500 ms   303900fffa00          MOVE.W ($FFFA00).L,D0
15, 1004D4:   7.518187 ms   00400300              ORI.W #$300,D0
17, 1004D8:   7.518562 ms   33c000fffa00          MOVE.W D0,($FFFA00).L
20, 1004DE:   7.519250 ms   08f9000e00fffa04      BSET #$e,($FFFA04).L
26, 1004E6:   7.520250 ms   103900fffa17          MOVE.B ($FFFA17).L,D0
30, 1004EC:   7.520937 ms   000000F0              ORI.B #$F0,D0
32, 1004F0:   7.521312 ms   13c000fffa17          MOVE.B D0,($FFFA17).L
36, 1004F6:   7.522000 ms   08b9000700fffa21      BCLR #$7,($FFFA21).L
```

```
Auto_Kathy_p ->Union2.U_Int2 long 1 (0x
Buffer char [80] size 80 bea "\0\0\0\0
Auto_Kathy_p struct .KATHY *C3E
Auto_Kathy_p ->Int1 long 1 (0x1)
y long -1431655750 (0xaaaaaaba)
x long -1464161553 (0xa8baaaef)
```

```
value_to_s(struct .KATHY *C3E )
toggle_case(char *C3E )
main()
```

```
Select a register to edit, then hit <Enter> or doubleclick or type new value directly.
```

FEATURES

- Supports both the 683xx and 68HC16 families.
- User Interface under Microsoft Windows.
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8051 68HC11

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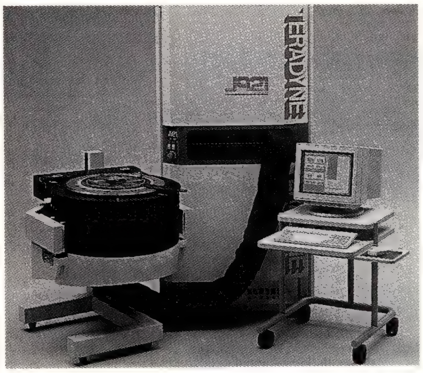
CIRCLE 167 FOR U.S. RESPONSE

CIRCLE 168 FOR RESPONSE OUTSIDE THE U.S.

▼ ASIC TESTER COMBINES PERFORMANCE, ECONOMY

The J921 VLSI production test system targets high-performance ASICs. The system can handle devices with up to 512 I/O pins, and operates at frequencies to 150 MHz, with data rates to 300 MHz and edge-placement accuracy to ±300 ps. A scan-path option is available. The J921 achieves high performance and economy with a design that aims specifically at ASIC test rather than more general IC testing. For example, a Palette-Per-Pin timing system permits on-the-fly switching of device timing values without the more costly timing generators used in conentional VLSI testers. A J921 configured for devices with up to 256 pins starts at about $1.2 million, Typical delivery is in 16 to 18 weeks.



Teradyne Inc.
Semiconductor Test Div.
30801 Agoura Hills Rd.
Agoura Hills, CA 91301
(818) 991-2900
▶CIRCLE 505

▼ SBUS I/O BOARD DOES 25-MFLOPS PROCESSING

The SB-A2200 plug-in board for Sun Sparcstations offers two 16-bit analog inputs and two analog outputs along with 25 MFLOPS of processing power. Two input channels attenuate input signals 90 dB in one-sixth octave. A 93-dB signal-to-noise ratio, –95-dB total harmonic distortion, and ±0.050 amplitude flatness allow high-accuracy acquisition from dc to 22 kHz. An on-board AT&T DSP3210 digital signal processor runs at 50 MHz and has 2 kwords of fast on-chip SRAM, 128 kwords of fast SRAM, or 512 kwords of psuedo-SRAM. The board comes with NI-DSP, a DSP library of functions for ANSI C compilers for Solaris 1.X and 2.X; NI-DAQ, a library of functions for Sbus-based acquisition boards; and SpectrumWare, a virtual instrument for dynamic signal acquisition and analysis, including total harmonic distortion and frequency response. The SB-A2200 costs $2495.

National Instruments Inc.
6504 Bridge Point Pkwy.
Austin, TX 78730-5039
(800) 433-3488
(512) 794-0100
▶CIRCLE 506

FUNCTION GENERATORS

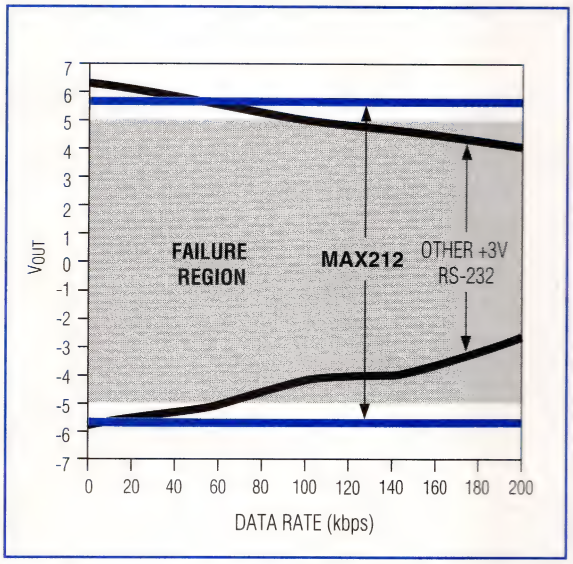
Manufacturer	Model/ Price	Frequency range	Type of functions (waveforms)	Type of internal sweep	Type of internal modulation	Max. output (V p-p into 50 ohms)	Remarks
Kenwood Communications Corp. Test and Measuring Instruments Group P.O. Box 22745 2201 E. Dominguez St. Long Beach, CA 90801-5745	FG-272/ $349	0.2 Hz - 2 MHz	Sine, square, ramp, pulse, TTL	Linear	—	10	Voltage-controlled frequency function; dc offset.
	FG-273/ $449	0.2 Hz - 2 MHz	Sine, triangle, square, ramp, pulse, TTL, CMOS	Linear, logarithmic	—	10	Includes 10-MHz counter; voltage-controlled frequency function; dc offset.
Krohn-Hite Corp. 255 Bodwell St. Avon, MA 02322 (508) 580-1660	1000A/ $650	0.2 Hz - 3 MHz	Sine, triangle, square, TTL, control voltage	—	—	10	External VCO input.
	1200A/ $695	0.2 Hz - 3 MHz	Sine, triangle, square, ramp, TTL, control voltage	Linear	—	10	External VCO input, ±10-V dc offset.
	1400A/ $1095	0.2 Hz - 3 MHz	Sine, triangle, square, ramp, pulse	Linear	—	10	Modes include gate, trigger, pulse sweep, trigger sweep, gated sweep, tone-burst; ±10-V dc offset, external VCO input.
	1600A/ $1195	0.2 Hz - 3 MHz	Sine, triangle, square, ramp, pulse	Linear, logarithmic	—	10	Same as 1400A.
	2000/ $1495	3 mHz - 30 MHz	SIne, triangle, square, ramp, pulse, TTL	—	—	15	External VCO input; variable symmetry; ±15-V dc offset.
	2200/ $1895	3 mHz - 30 MHz	Sine, triangle, square, ramp, pulse, TTL	Linear, logarithmic	—	15	External VCO input; ±15-V dc offset; gate, trigger, burst modes.
	2400/ $1995	3 mHz - 30 MHz	Sine, triangle, square, ramp, pulse	Linear	AM, FM, phase lock	15	Auxiliary 0.3 Hz - 300-kHz generator; gate, trigger, dual-phase operation.
	5900C/ $2445	100 μHz - 5 MHz	Sine, triangle, square, sawtooth, pulse	Linear, logarithmic	—	15	External VCO input; variable symmetry, dc offset; 1000-step autoprogrammer.

TRUE +3V RS-232 IC REDUCES POWER 8 TIMES!

Complete Serial Port Runs at 120kbps & Drives a Mouse @ 3.0V!—GUARANTEED

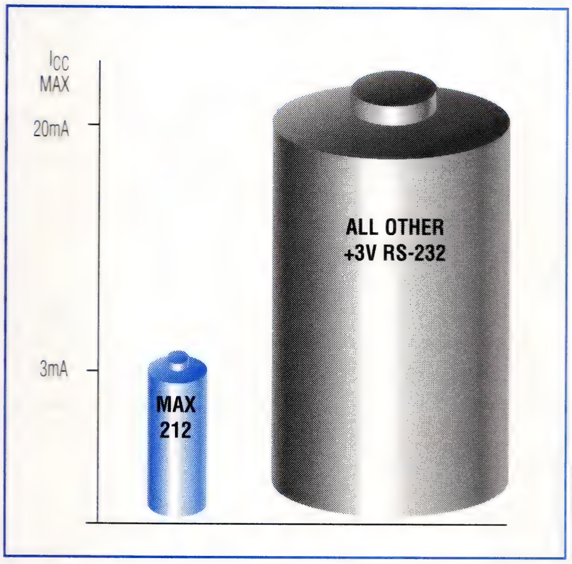
Maxim's new MAX212 has the highest data rate and the lowest power of any 3V RS-232 IC. And, the MAX212 is the only +3V RS-232 transceiver powerful enough to drive a mouse at 3.0V!

120kbps DATA RATE—GUARANTEED!



A regulated output stage guarantees RS-232 output levels are met; even at 120kbps!

REDUCE POWER 8 TIMES!



The MAX212's proprietary architecture reduces power 8 times!

Select the Low Power +3V RS-232 Transceiver for Your Design

Part	ICC (max)	Data Rate	RX Active in Shutdown	Description
MAX212	**3.0mA**	**250**	**5**	**True RS-232 From +3.0V**
MAX560	8mA	120	2	Meets Low Power EIA/TIA-562
MAX561	8mA	120	0	Pin Compatible with MAX241

INTERFACE ANALOG DESIGN GUIDE 2

Data Sheets • Applications Notes • Free Samples

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+5V CMOS RS-232 ICs Survive ±10kV ESD Strikes—Guaranteed!

I/O Port Resistant to ESD with No Latchup

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CIRCLE 151 FOR U.S. RESPONSE

CIRCLE 152 FOR RESPONSE OUTSIDE THE U.S.

FUNCTION GENERATORS

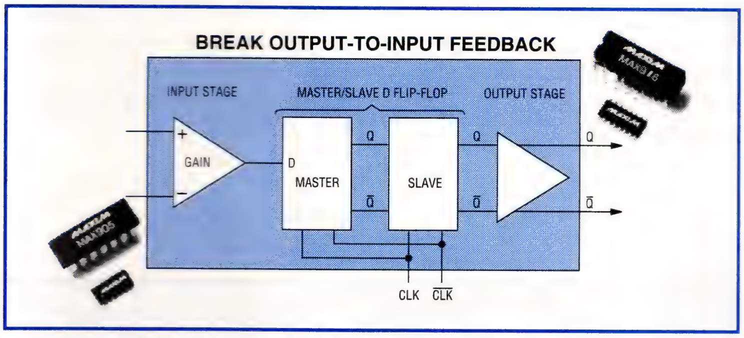
Manufacturer	Model/ Price	Frequency range	Type of functions (waveforms)	Type of internal sweep	Type of internal modulation	Max. output (V p-p into 50 ohms)	Remarks
Krohn-Hite Corp. 255 Bodwell St. Avon, MA 02322 (508) 580-1660	5920/ $2995	100 μHz - 5 MHz	Sine, triangle, square, sawtooth, pulse, arbitrary	Linear, logarithmic	—	15	Same as 5900C plus 16-kpoint, 4000-count resolution arbitrary capabililty.
	2100A/ $4495	10 mHz - 31.16 MHz	Sine, triangle, square, linear ramp, exp. ramp, ±pulses	Linear, logarithmic	—	15	External VCO input; 0.5 ppm accuracy std., 0.1 ppm opt.; 0.025-dB amplitude flatness.
Leader Intruments Corp. 380 Oser Ave. Hauppauge, NY 11788 (800) 645-5104 (516) 231-6900	LFG-1300S/ $575	0.02 Hz - 2 MHz	Sine, triangle, square, sawtooth, pulse, TTL, dc	Linear, logarithmic	—	10	AM, VCO inputs.
	LFG-1310/ $1245	0.01 Hz - 10 MHz	Sine, triangle, square, pulse, TTL, haversine	Linear, logarithmic	—	10	Symmetry controls for waveshape, sweep; CW, trigger, gate, burst, sweep modes.
H. C. Protek Inc. P.O. Box 59 154 Veterans Dr. Norwood, N.J. 07648 (201) 767-7242	B-801/ $215	0.02 Hz - 2 MHz	Sine, triangle, square, pulse, ramp, slewed sine	Linear	—	8	—
	B-810/ $749	0.01 Hz - 10 MHz	Sine, triangle, square, pulse, ramp, slewed sine, TTL	Linear, logarithmic	AM	20 V (open)	Built-in counter.
Racal-Dana Instruments Inc. 4 Goodyear St. Irvine, CA 92718 (800) 722-3262 (714) 859-8999	6060-6061/ $4000	0 - 30 kHz	Sine, triangle, square, arbitrary	—	—	1	C-size VXI modules; 8 or 16 channels; also has 32 digital channels.
Stanford Research Systems 1290D Reamwood Ave. Sunnyvale, CA 94089 (408) 744-9040	DS335/ $995	1 μHz - 3.1 MHz	Sine, triangle, square, ramp, white noise	Linear, logarithmic	FSK	10	Direct digital synthesis; external FSK; IEEE-488, RS-232 opt.
	DS340/ $1595	1 μHz - 15.1 MHz	Sine, triangle, square, ramp, white noise, arbitrary	Linear, logarithmic	FSK	10	Direct digital synthesis; external FSK; IEEE-488, RS232, waveform-generation software opt.
	DS345/ $2195	1 μHz - 30.2 MHz	Sine, triangle, square, ramp, white noise, arbitrary	Linear, logarithmic	AM, FM, phase burst	10	Direct digital synthesis; external AM; IEEE-488, RS-232, waveform-generation software opt.
Tabor Electronics Inc. 25 Rutgers Ave. Cedar Grove, NJ 07009 (201) 239-0425	8020/ $1495	2 mHz - 20 MHz	Sine, triangle, square, dc	Linear, logarithmic	FM	15	IEEE-488 std.
	7223PC/ $1695	10 mHz - 50 MHz	Sine, square, ramp, pulse (inc. exp. and gaussian), noise dc	—	—	12	PC plug-in card; 2-channels; built-in sequencer.
	8021/ $1795	2 mHz - 20 MHz	Sine, triangle, square, ramp, pulse	Linar logarithmic	FM, PWM	15	IEEE-488 std.
	8550/ $2495	10 mHz - 50 MHz	Sine, triangle, square, TTL, dc	Linear, logarithmic	AM, FM	16	IEEE-488 std.
	8551/ $2995	10 mHz - 50 MHz	Sine, triangle, square, ramp, pulse, TTL	—	AM, FM, PWM	16	Rise/fall time control; IEEE-488 std.
	8553/ $4000	10 mHz - 50 MHz	Sine, triangle, square, arbitrary	Linear, logarithmic	AM, FM	16	Includes waveform-generation sofrtware.
Tektronix Inc. P.O. Box 1520 Pittsfield, MA 01202 (800) 426-2200	CFG250/ $395	0.1 Hz - 100 kHz	Sine, triangle, square, pulse, TTL	(User defined)	—	10	±5 V dc offset; UL, CSA, VDE certified; variable duty cycle.
	CFG253/ $445	1 Hz - 10 MHz	Sine, triangle, square, pulse, TTL	(User defined)	—	10	Same as CFG253.

2ns COMPARATORS RESOLVE 3mV SIGNALS WITH NO OSCILLATION

Propagation Delay Independent of Overdrive

Maxim's new MAX905/MAX906 and MAX915/MAX916 are the first ultra high-speed, precision, single and dual ECL and TTL compatible comparators to eliminate oscillation caused by unwanted parasitic feedback. Unlike other comparators, the master/slave architecture resolves input voltages as small as 2mV (MAX915) to 3mV (MAX905) over its common-mode range, and propagation delay is independent of input overdrive. *No dispersion!** This eliminates synchronization problems common with industry standard comparators.

- ◆ **Immune to Oscillation**
- ◆ **2ns Propagation Delay (MAX905/MAX906)**
- ◆ **Single or Dual Supply Operation**
- ◆ **7.9V Input Voltage Range Includes Negative Rail**



Master/slave D-flip/flop prevents oscillation and resolves signals as low as 3mV.

Choose From Maxim's Special-Function Comparator Solutions

	Device	Description	Comparators per pkg	Logic	Prop Delay (ns)	Input Resolution	No Dispersion*	Single-Supply Capability
	MAX905	Edge-triggered Master/Slave Architecture	Single	ECL	2	3mV	✓	✓
	MAX906	Dual MAX905	Dual	ECL	2	4mV	✓	✓
NEW	MAX915	Edge-triggered Master/Slave Architecture	Single	TTL	6	2mV	✓	✓
NEW	MAX916	Dual MAX915	Dual	TTL	6	3mV	✓	✓
	MAX910	8-bit Digital Threshold Control	Single	TTL	8	10mV		
	MAX911	8-bit Digital Threshold Control	Single	ECL	4	10mV		

**Dispersion is the change in propagation delay from 3mV to 1V input overdrive.*

1.2µA Single & Dual Op Amps!

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CIRCLE 153 FOR U.S. RESPONSE **CIRCLE 154 FOR RESPONSE OUTSIDE THE U.S.**

▼ FUNCTION GENERATOR HAS 1% SINE-WAVE DISTORTION

The Model 2006 sweep-function generator features less than 1% sine-wave distortion from 10 Hz to 200 kHz, with an overall frequency range of 0.2 Hz to 2 MHz. Besides sine waves, the unit outputs square, triangle, ramp, and TTL functions. Sweep outputs are possible using an external VCO signal or the internal rate and width controls, which allow independent control of the sweep width up to 100:1 and of the sweep rate from 15 ms to 2.5 seconds. A time-symmetry control creates duty cycles from 20% to 50%. The maximum amplitude of 10 V p-p into 50 Ω can be attenuated with a fixed 30-dB attenuator. A dc offset is adjustable from –5 to +5 V into a 50-Ω load. The Model 2006 retails for $279.95 and is available from stock.

Global Specialties
70 Fulton Terr.
New Haven, CT 06512
(800) 572-1028
▶ CIRCLE 507

▼ BER TESTER HANDLES 12-GBIT/S SYSTEMS

The HP 71612A bit-error-rate (BER) tester system includes pattern generators, error detectors, and error performance analyzers needed to address the growing number of high-speed digital applications at up to 12 Gbits/s. The system's high speed and 8-Mbit user-programmable pattern size allow simulation of multiple Sonet and SDH frames at the STS-192 and STM-64 (9.953 Gbits/s) transmission rate. Margin testing of systems carrying line rate overhead can be made to 12 Gbits/s. An error location analysis (ELA) option helps identify the cause of pattern-dependent errors. The HP 71612A costs $399,600, and the ELA option costs $33,300. Delivery is in 12 weeks.

Hewlett-Packard Co.
Direct Marketing Organization
P.O. Box 58059
MS51L-SJ
Santa Clara, CA 95051-8059
(800) 452-4844
▶ CIRCLE 508

▼ UNIT ANALYZES DIGITAL MODULATION TO 2.7 GHZ

The ME2627B Digital Modulation Signal Analyzer has a frequency range of 10 MHz to 2.7 GHz, making it suitable for testing digital cellular and digital cordless telephones. The system can analyze and measure digital modulation parameters like frequency, phase error, modulation accuracy, and amplitude envelope. It supplies $\pi/4$ DQPSK and GMSK modulated signals, and can change measuring conditions, filter type, sampling points, and display. Results can be displayed in various forms, including spectrum analyzer, eye-pattern, constellation, and trellis. The input level range is –10 to +20 dBm; phase error accuracy is less than 1° rms and less than 4° peak; frequency error is less than 5 Hz at 1 GHz. The ME2627B costs $125,778.

Anritsu Wiltron Sales Co.
685 Jarvis Dr.
Morgan Hill, CA 95037-2809
(408) 776-8300
▶ CIRCLE 509

FUNCTION GENERATORS

Manufacturer	Model/ Price	Frequency range	Type of functions (waveforms)	Type of internal sweep	Type of internal modulation	Max. output (V p-p into 50 ohms)	Remarks
Tektronix Inc. P.O. Box 1520 Pittsfield, MA 01202 (800) 426-2200	CFG280/ $995	0.1 Hz - 11 MHz	Sine, triangle, square, pulse, TTL	(User defined)	AM, FM	10	Includes 100 MHz frequency counter.
	AFG5102/ $3995	20 mHz - 20 MHz	Sine, triangle, square, ramp, pulse, dc, arbitrary	Liner logarithmic	AM, FM	15	Variable symmetry; burst mode; module for TM5003 or TM5006 mainframe.
	AFG2020 $7995	0.5 Hz - 100 MHz	Sine, triangle, square, ramp, pulse, noise, dc, arbitrary	Linear, logarithmic	AM, FM, FSK, PSK	10	Direct digital synthesis; waveform display and graphical user interface; IEEE-488 std.
Wavetek Corp. Instruments Div. 9045 Balboa Ave. San Diego, CA 92123 (619) 279-2000	19/ $395	2 mHz - 2 MHz	Sine, triangle, square, dc	Linear, logarithmic	AM	10	VCO input
	75/ $1695	50 mHz - 5 MHz	Sine, triangle, square, ramp, haversine, dc	—	—	5	—
	23/ $2595	10 mHz - 12 MHz	Sine, triangle, square, ramp, haverwaves, dc	—	—	10	VCO input, AM with external signal.
	80/ $2695	10 mHz - 50 MHz	Sine, triangle, square, pulse, dc	Linear, logarithmic	—	16V	VCO, AM, FM with external signal.
	1370/ $2695	10 mHz - 12 MHz	SIne, triangle, square, dc	Linear, logarithmic	—	10 V	VXI module; VCO input.
	395/ $3395	1 mHz - 50 MHz	Sine, triangle, square, ramp, pulse, dc, noise, (sin X)/X, haver-sine, arbitrary.	Linear, logarithmic	—	10 V	AM with external signal.

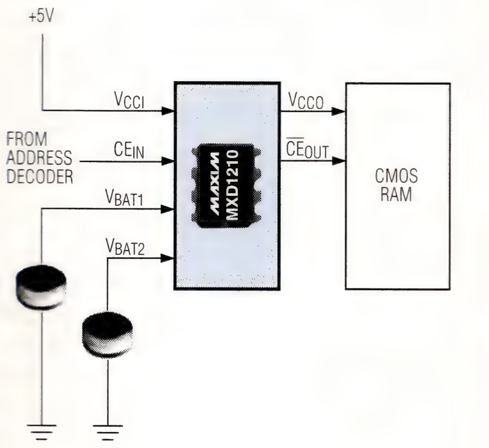
RAM PROTECTION IC CONSUMES ONLY 230µA

Write Protection & Battery Backup in an 8-pin SOIC

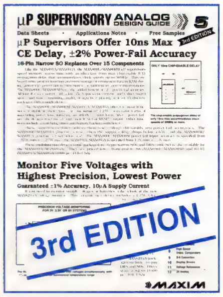
The MXD1210 converts CMOS RAM into nonvolatile memory by connecting the higher of two backup batteries to the RAM V_{CC} during power failures. By gating the RAM's enable signal $\overline{CE}$, the MXD1210 prevents spurious write operations during power failures.

- **Low I_{SUPPLY} –**
  - **230µA in Operating mode**
  - **2nA in Backup mode**
- **Backup Switchover With Redundant Battery Option**
- **20ns max Chip Enable Prop Delay**
- **5% or 10% power fail trip thresholds**
- **Smallest package – 8-pin SOIC**
- **Second-source to DS1210 available in 8-pin DIP or 10-pin SOIC**

CONVERT RAM TO NONVOLATILE MEMORY



Like the DS1210, the MXD1210 provides backup-switchover and chip-enable gating. But power consumption is 10X lower, and the 8-pin SOIC package is only 1/4 the size of the DS1210 16-pin SOIC.



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CIRCLE 155 FOR U.S. RESPONSE CIRCLE 156 FOR RESPONSE OUTSIDE THE U.S.

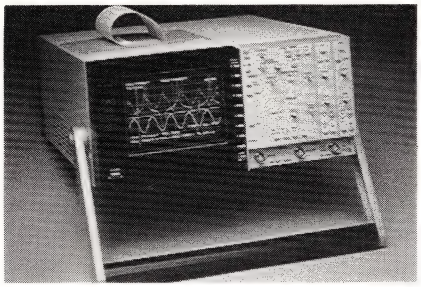
▼ BOARD TESTERS OFFER WIDE PERFORMANCE RANGE

A six-member family of board testers offers users a wide range of choices to accommodate various levels of board complexity and different test strategies. The series includes three performance levels, each with two systems: one aimed at small to midsize boards (256-1920 pins) and one for midsize to large-scale boards (640-3840 pins). The testers handle analog, digital, mixed-signal, and memory testing tasks. The Combo I level testers do traditional in-circuit tests, while the Combo II level units perform combinatorial testing. The Xtended Performance systems do performance combinatorial testing. The first two levels feature clock speeds and synchronization frequencies to 20 MHz and driver/sensor memories of 16 kvectors. The Xtended Performance models run to 50 MHz and have 32-kvector memories. Prices start below $100,000.

GenRad Inc.
300 Baker Ave.
Concord, MA 01742-2174
(508) 369-4400
▶CIRCLE 620

▼ BACKLIT LCD DISPLAY HIGHLIGHTS 200-MHZ DSO

A 6-in. (diagonal) backlit color LCD screen delivers a bright, clear display of signals, text, cursors, and graticules on the Model 500 digital storage oscilloscope. The 2-channel scope offers a 200-MHz analog bandwidth for repetitive signals and a 200-Msample/s sampling rate for transient capture. Waveform-processing capabilities include pulse-parameter calculations on live or stored traces, averaging, limit testing, analysis and post-storage signal filtering, and mathematical operations. Data can be output to printers, plotters, or computers. IEEE-488 and RS-423 interfaces are standard. The Model 500 costs $3995, and an optional internal plotter goes for $495. Delivery is in 6 weeks.



Gould Inc.
Test & Measurement Group
8333 Rockside Rd.
Valley View, OH 44125
(216) 328-7000
▶CIRCLE 621

▼ FAST I/O DEVICE USES ENHANCED PARALLEL PORT

The DaqBook/200 offers 16-bit, 100-kHz data acquisition and 500-kbyte/s bidirectional communications with a notebook PC through the computer's enhanced parallel port (EPP). As an enhanced version of the standard Centronics-type parallel port, the EPP supplies true bidirectional, high-speed communication between the PC and the external DaqBook/200. The device also supports standard parallel ports. The DaqBook/200 has 16 analog-to-digital channels, 2 digital-to-analog channels, 24 digital I/O channels, 16 high-speed digital inputs, and 5 counter-timer channels. It comes with DaqView2, a Windows-based data-acquisition software package that saves acquired data directly to disk or seamlessly transmits it to other Windows applications. Also included is a programmable-gain input amplifier. The DaqBook/200 costs $1995. Delivery is within two weeks.

IOtech Inc.
25971 Cannon Rd.
Cleveland, OH 44146
(216) 439-4091
▶CIRCLE 622

▼ SIGNATURE ANALYZERS DO AUTOMATED TESTS

A pair of analog signature analyzers use a powerful signature digitization technique to automate the fault-finding function. The T4040 and T4080 offer 40 and 80 test channels, respectively. Three test modes include automated test, which compares a faulty module with a previously captured known-good signature. Also, dual-port operation compares a bad board with a known-good board, using either automated diagnosis or a visual display of the signatures. Lastly, conventional manual operation allows interactive probing and visual signature analysis. The units feature a virtual instrument interface, with control and display provided by any standard VGA-compatible PC over a serial link. The T4040 costs $3750, and the T4080 costs $4750.

Polar Instruments
522 Sprague Valley Dr.
Sumas, WA 98295
(206) 599-1430
▶CIRCLE 623

▼ TRAINING KIT TEACHES BOUNDARY-SCAN METHODS

A boundary-scan training kit, called the proTEST Training Kit, allows designers to become familiar with boundary-scan test techniques before producing their own target. The kit includes a target board, a boundary-scan controller, test-development tools, exercises, and a tutorial. Users can write tests for the training target, which is a known-good board containing boundary-scan circuitry. The tools in the kit are similar to those that come with the proTEST Test Development Systems. The tests are executed in hardware by the ScanJack boundary-scan controller, which plugs into the parallel port of any DOS-compatible personal computer. The proTEST Training Kit is priced at $995 in the U.S. and slightly higher in Asia and Europe. Delivery is in 30 days.

Alpine Image Systems Inc.
821 Riverside Dr.
Los Altos, CA 94024
(415) 941-3247
▶CIRCLE 624

▼ BENCHTOP DMMs OFFER HIGH DC ACCURACY

A pair of benchtop digital multimeters offer 4.5-digit resolution with 0.05% accuracy for measurements to 200 V dc. The DM-342B and DM-343B measure voltage to 1000 V dc and 750 V ac, current to 10 A ac and dc, resistance to 20 MΩ, and frequency to 200 kHz. Other features include data hold, diode check, continuity test, transistor H_{fe} check, and battery test. The DM-343B also includes true rms measurements, a relative mode, min/max recording, and an RS-232C interface. An IEEE-488 interface is optional. The DM-342B costs $199.95, and the DM-343B goes for $279.95.

Goldstar Precision Co. Ltd.
13013 E. 166th St.
Cerritos, CA 90701
(310) 404-0101
▶CIRCLE 625

NO SUBHARMONIC NOISE! 94% EFFICIENT DC-DC STEP-DOWNS POWER WIRELESS SYSTEMS

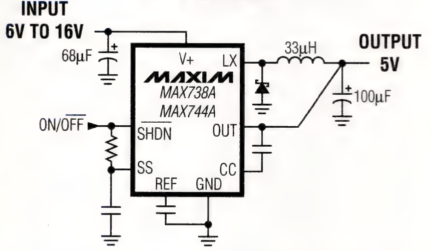
Internal Switches and Surface-Mount Packages Save Space

Compact size, battery-saving features, and low-noise make this new family of pulse-width modulated (PWM) step-down DC-DC converters ideal for portable communications and wireless applications. These drop-in replacements for Maxim's popular MAX730-family deliver up to 50% more output current, are free of subharmonic switching noise, maintain up to 94% efficiency, and are lower priced. And, the MAX744A has guaranteed 159kHz to 212.5kHz oscillator limits to avoid interference in the sensitive 455kHz IF band. External component selection has already been optimized to simplify design work.

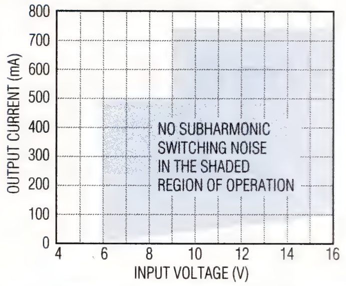
- **No Subharmonic Switching Noise with Low V_{IN}-V_{OUT} Differentials**
- **88% - 94% Efficiency**
- **Compact SOIC Footprint**
- **Up to 750mA Output Currents, Guaranteed**
- **Logic-Controlled 6μA Shutdown**
- **5V, 3.3V, or Adjustable Outputs (1.25V to V_{IN})**
- **Evaluation Kits Available†**

DEVICE	REPLACES	OUTPUT VOLTAGE	INPUT RANGE	PRICE*
MAX730A	MAX730	5V	5.2V–11V	$2.15
MAX738A	MAX738	5V	6V–16V	$2.60
MAX744A	NEW	5V	6V–16V	$2.90
MAX748A	NEW	3.3V	3.3V–16V	$2.60
MAX763A	NEW	3.3V	3.3V–11V	$2.15
MAX750A	MAX750	ADJ	4V–16V	$2.15
MAX758A	MAX758	ADJ	4V–11V	$2.60

LOW-NOISE, COMPACT STEP-DOWN IS 94% EFFICIENT

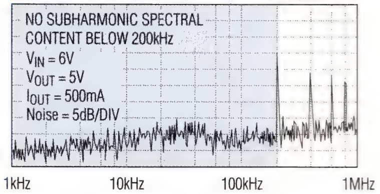


NO SUBHARMONIC NOISE OVER WIDE OPERATING RANGE



The MAX744A exhibits no subharmonic switching noise over a wide input voltage and output current range.

SPECTRAL ANALYSIS OF MAX744A OUTPUT VOLTAGE NOISE vs. FREQUENCY



The MAX744A output voltage noise spectra shows no switching noise below the 200kHz fundamental switching frequency.

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*1000up, US recommended resale, commercial temperature range PDIP devices.

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† Order MAX738EVKIT-DIP or MAX738EVKIT-SO and appropriate free sample.

CIRCLE 157 FOR U.S. RESPONSE   CIRCLE 158 FOR RESPONSE OUTSIDE THE U.S.

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▼ REMOTE NETWORK MONITOR HELPS WITH DIAGNOSTICS

The IDMS-3013 Remote Segment Monitor is the first offering in the Internetwork Diagnostics & Monitoring System (IDMS) family. The instrument implements all nine standard functional groups of the Remote Monitoring Management Information Base. Data gathered includes packet counts; collision, error, and broadcast rates; and the top 10 talkers and error producers. User-defined data captures provide historical information for trend analysis and network planning. A graphical user interface displays all results as tables, graphs, or dials. The unit can run as a standalone management station or with SunConnect's SunNet Manager. Other platforms will be supported in the future. The IDMS-3013 is priced at $2800; the IDMS Manager software costs $3500.

Wandel & Goltermann
Technologies Inc.
1030 Swabia Ct.
Research Triangle Park,
NC 27709
(919) 941-5730
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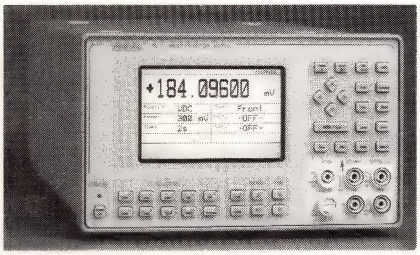
▼ MULTIFUNCTION METER DOES DATA ACQUISITION

The 8017 multifunction meter makes a number of standard measurements, and can perform controlled-measurement data acquisition with an optional 80-channel scanner. The unit measures ac and dc voltage and current, 2-wire and 4-wire resistance, frequency, period, and temperature (using platinum-tipped probes or thermal elements). The ac readings are determined simultaneously as true effective values and pure peak and average values, including crest factor. Resolution is 7.5 digits. Sample times can be set between 1 ms and 100 seconds. The unit can store 100,000 measurement values per sampling sequence. An IEEE-488, RS-232, and Centronics interface are built in. The 8017 costs $3600. The optional scanner is $1200.



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4650 Arrow Hwy.
Bldg. E-5
Montclair, CA 91763-1217
(800) 441-0305
(909) 621-7292
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▼ SIMULATOR EMULATES ESCON DEVICES

The ChannelScope 9120 simulator is a development and testing instrument for Enterprise Systems Connection (ESCON) products. Users can program the simulator to emulate an ESCON host channel, control unit, or director. The unit allows designers to write, compile, debug, execute, and analyze the results of test cases from a single, integrated menu that complies with the Systems Application Architecture standard. The simulator consists of an EISA-based pc board and DOS-based software. The product comes either installed in a PC or as a board set and software to be installed in the user's PC. The 9120 costs $37,500 without a PC and is available immediately.

McData Corp.
310 Interlocken Pkwy.
Broomfield, CO 80021
(800) 545-5773
(303) 460-9200
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▼ PROGRAMMER/TESTER RUNS 32 PCMCIA CARDS

The CardServer-32TX can simultaneously read, write to, test, and functionally exercise up to 32 PCMCIA cards simultaneously. The unit supports all types of 68-pin PC (IC) cards, including those compatible with PCMCIA 2.0 and JEIDA 4.1 (Type I, II, and III), Intel ExCA, and ATA interface solid-state and rotating media cards. All implementation technologies—flash, SRAM, OTP, EEPROM, and mixed—are supported. Programming and verification of 32 Intel 1-Mbyte flash cards is performed in about 13 seconds. Users can run the device in standalone mode or remotely over a computer network. The system's software runs under Windows and accommodates a variety of pointing devices, including a touch-screen monitor. CardServer-32TX prices range from $9950 to $19,950.

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▼ I/O BOARDS FEATURE ON-BOARD INTELLIGENCE

The DAP 1216e and DAP 2415e data-acquisition processors are PC plug-in boards that combine 16-bit analog-to-digital and digital-to-analog conversions with on-board intelligence. The boards feature DAPL, a dedicated multitasking real-time operating system that runs on the board's own processor and communicates with the software running on the host PC. DAPL is optimized for data acquisition and has over 100 standard commands for on-board processing. Both boards have 16 analog inputs and 2 analog outputs. The DAP 2416e also contains its own digital-signal-processing hardware. The boards are available now at prices from $2495 to $3695.

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▼ DC POWER SUPPLIES HAVE DIGITAL METERS

The PMC-A series power supplies feature two digital meters for easy and independent output voltage and current monitoring. The supplies come in a voltage range of 0 to 18 V dc with current ranges of 0 to 1 A, 0 to 2 A, and 0 to 3 A, or a voltage range of 0 to 35 V dc with current ranges of 0 to 0.5 A, 0 to 1 A, and 0 to 2 A. The supplies can be linked in series to increase output voltage or in parallel to increase current. The use of 10-turn potentiometers provides excellent voltage and current resolution. Users can also control voltage and current remotely. A remote sensing capability compensates for voltage drops caused by load cable resistance. Prices for the PMC-A series start at $379.

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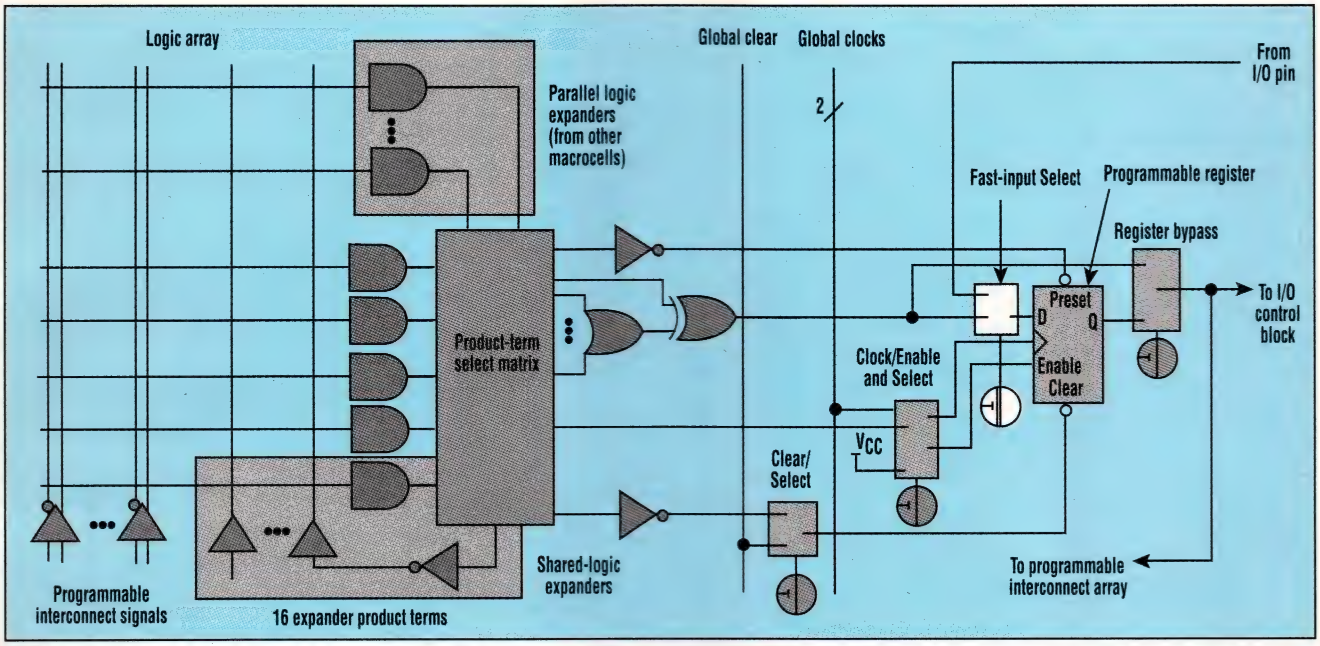


1. ADDING TWO GLOBAL CLOCKS and a fast-input select function helps accelerate the performance of Altera's MAX 7000E family of enhanced complex PLDs.

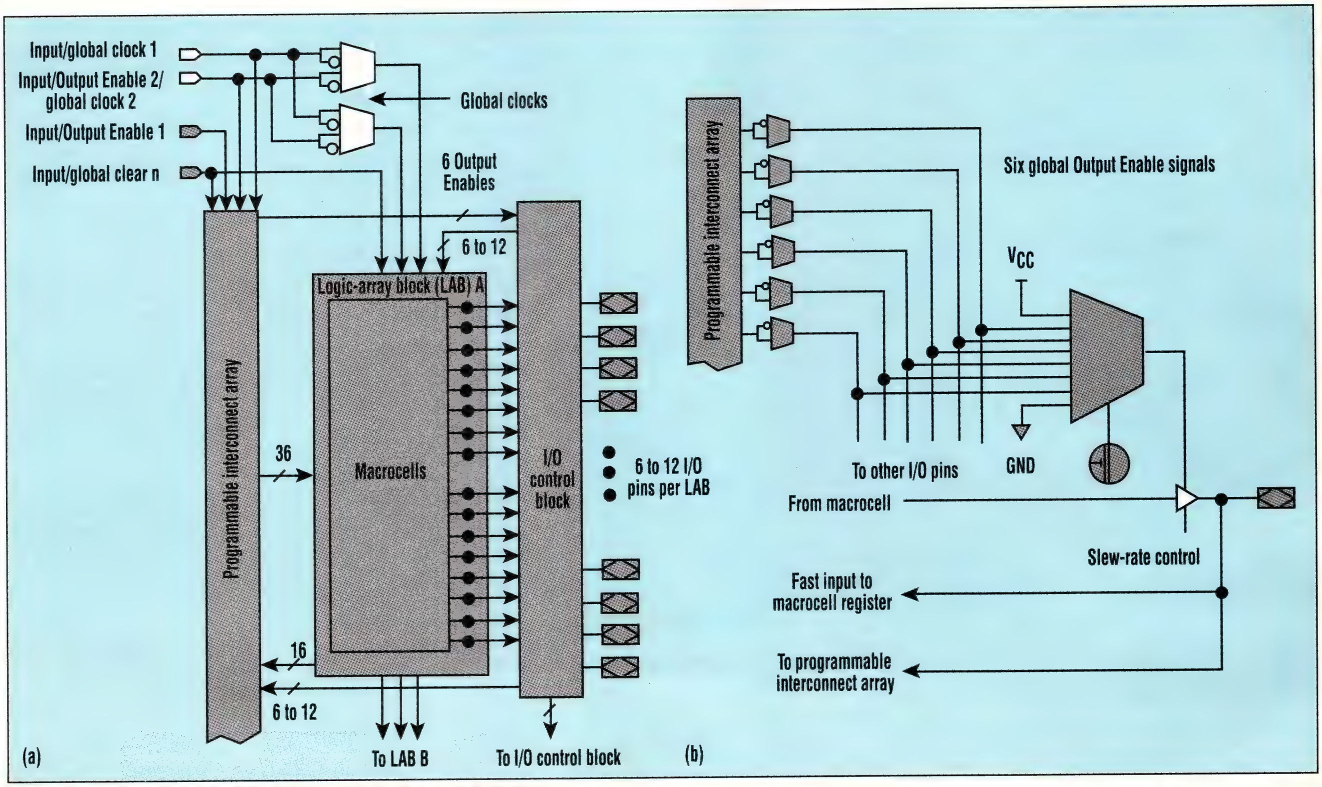
ENHANCED PROGRAMMABLE LOGIC SPEEDS UP SYSTEMS

DAVE BURSKY

Enhancements a company makes to an existing product family, through the use of finer-line processes, typically involve boosting an IC's clock speed or adding more gates. Designers at Altera, however, felt that an enhancement should go beyond that. This can be evidenced in the company's just-released MAX 7000E family of complex programmable-logic devices (PLDs), which provides architectural enhancements that improve the circuit performance of complex PLDs (shorter input-to-output delays), as well as augment routability and usability features.

Altera's designers paid closer attention to overall system performance, rather than concentrate on just shortening the basic input-to-output delays of the PLDs. Such an approach is critical, explains Sandeep Vij, technical product manager, since the complex PLD application focus seems to be shifting away from just peripheral control functions and instead embracing overall system functional integration. Thus, the architectural enhancements included in the 7000E family of complex PLDs help boost system performance by 60% and trim the input-to-output delays to just 10 to 12 ns.

A superset of the original MAX 7000 family, the four members of the 7000E series, include six logic-controlled Output Enable control signals, two high-speed global clocks, quick input paths to the on-chip macrocells, and short setup times (3 ns). Furthermore, all of the output lines have programmable output-slew-rate control to better match the signal speeds to the critical signal paths and to minimize



2. EACH OF THE TWO GLOBAL CLOCKS can have its true or complement phase directed to the macrocells (a). Array clocks also are still available to the macrocells. In addition, Altera included six global Output Enable signals that designers can select at each output macrocell (b). Each output can be used to either enable bus-control logic, activate or power down an off-chip function, or perform some other control function.

ground bounce on non-speed-critical output lines.

The four chips in the 7000E series have complexities of 128, 160, 192 and 256 macrocells with I/O pin counts of 160 pins (for the 128-, 160- and 192-cell chips) and 208 pins for the 256-cell chip. Each macrocell starts like the macrocells in the 7000 series, with the product-term matrix, parallel logic expanders, and 16 expander product terms as part of the shared-logic expander *(Fig. 1)*. Added to the cell, though, are two selectable global clock lines and a fast-input Select block.

DIRECT ROUTING

With the fast-input selector, users can directly route a signal from an I/O pin to the macrocell register's input, which shortens the signal delay path. That shorter path improves the chip-to-chip communication paths, reducing the chip-to-chip delays and permitting higher system operating frequencies.

For example, a multi-clock bus interface can run at a frequency of 76 MHz, up from about 55 MHz for the original 7000 family, while a digital-video image controller can clock at a frequency of 62 MHz—a 63% improvement over the 7000 series. The macrocell product terms, though, can still be used as parallel expanders and the core macrocells can function as input registers.

By giving designers a choice of two global clock signals, each with programmable polarity as well as the array clock signals, circuit functions can be implemented to take advantage of two-phase clocking, synchronous bus interfaces, as well as control logic that needs short clock-to-output times *(Fig. 2a)*. The global clock lines, along with the other system enhancements, allow the chips to operate over a wide span of clock speeds ranging from a low of 28 MHz up to a high of 100 MHz, depending on the application.

Offering users more control of logic functions, the six programmable Output Enable signals can be used for multiprocessor bus control, direct microprocessor datapath interfaces, and other functions that require direct control. All six signals are routed to each I/O pin and individually selected at each pin through a programmable multiplexer *(Fig. 2b)*. The output signals can also perform some degree of function management by activating or powering down off-chip peripheral functions.☐

PRICE AND AVAILABILITY

The MAX 7000E family come in a wide range of packages, from 84-lead PLCCs for the 128- and 160-macrocell EPM7128E and 7160E, up to 208-lead PQFPs for the 256-macrocell EPM7256E. Price is $129.50 each in 100-piece quantities for the EPM7256E (20-ns speed), which is available the first quarter of next year. Samples of the 192- and 256-macrocell versions will be available next quarter, with samples slated for the second quarter of 1994.

Altera Corp., 2610 Orchard Pkwy., San Jose, CA 95134-2000; Erik Cleage, (408) 894-7000. **CIRCLE 511**

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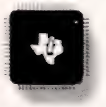

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TLC320AC01 At A Glance

- Low power consumption (100 mW) for portable systems
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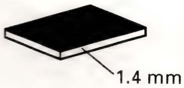
- Shrink quad flat packaging (SQFP) available for low-profile, portable applications 
- Single 5-V power supply for simplified system design
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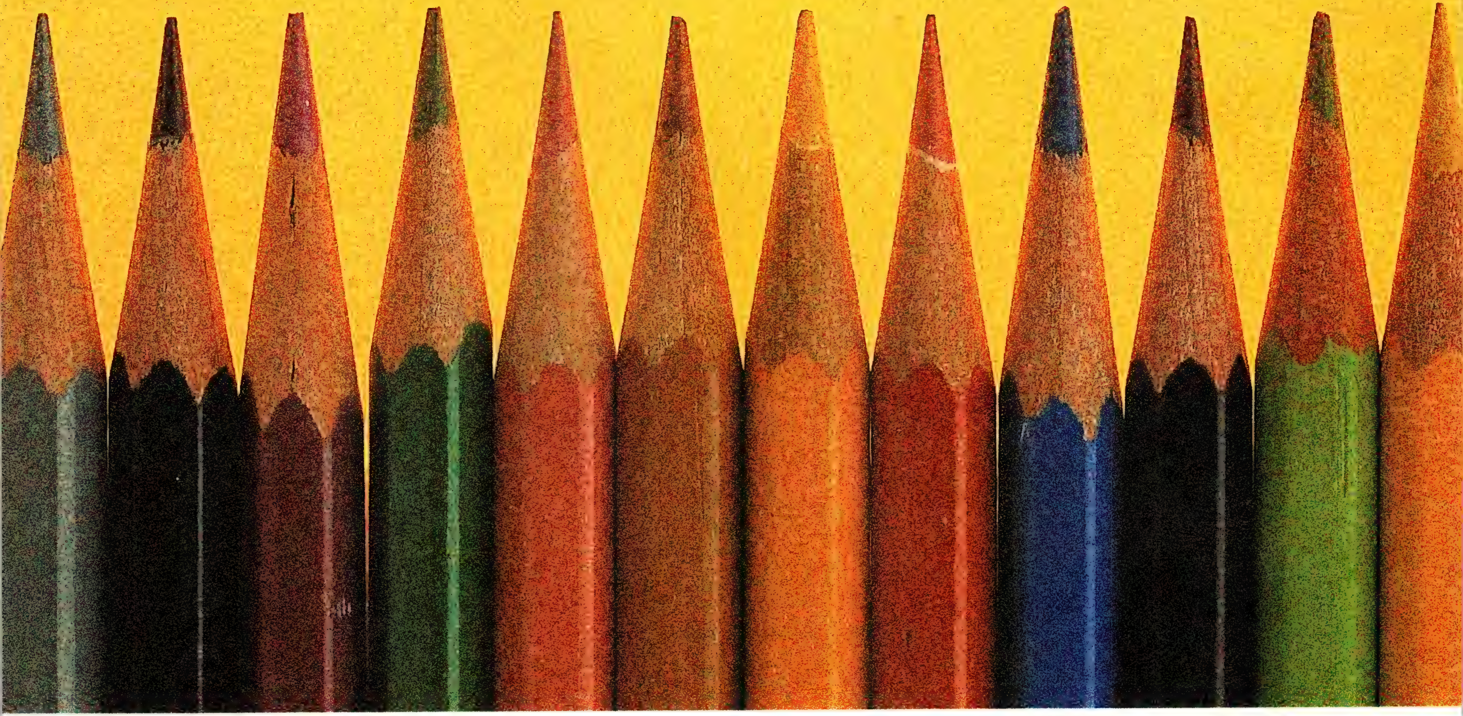

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					IDD1	IDD2	IDD5	IDD7
Standard	x 1/ x 4	HY514100 HY514400	300ml 20/26 SOJ	60/70/80	90mA	2mA	1mA	
		HY514100 A/AL HY514400 A/AL HY514410 A/AL	300ml 20/26 SOJ, TSOP-II, Reverse TSOP-II	50/60/70	110mA	1mA	200μA	300μA
Fast	x 1/ x 4	HY534100/L HY534400/L HY534410/L	300ml 20/26 SOJ, TSOP-II, Reverse TSOP-II	40/50/60	120mA	1mA	75μA	200μA
Wide-Bit	x 8	HY524800	350ml 28 SOJ	70/80	135mA	2mA	1mA	—
		HY514800/L/LS HY514170/L/LS HY514260/L/LS	400ml 28 SOJ, TSOP-II	60/70/80	170mA	2mA	200mA	300μA
	x 16		400ml 40 SOJ 44 TSOP-II					

* Note These specs can be changed during development

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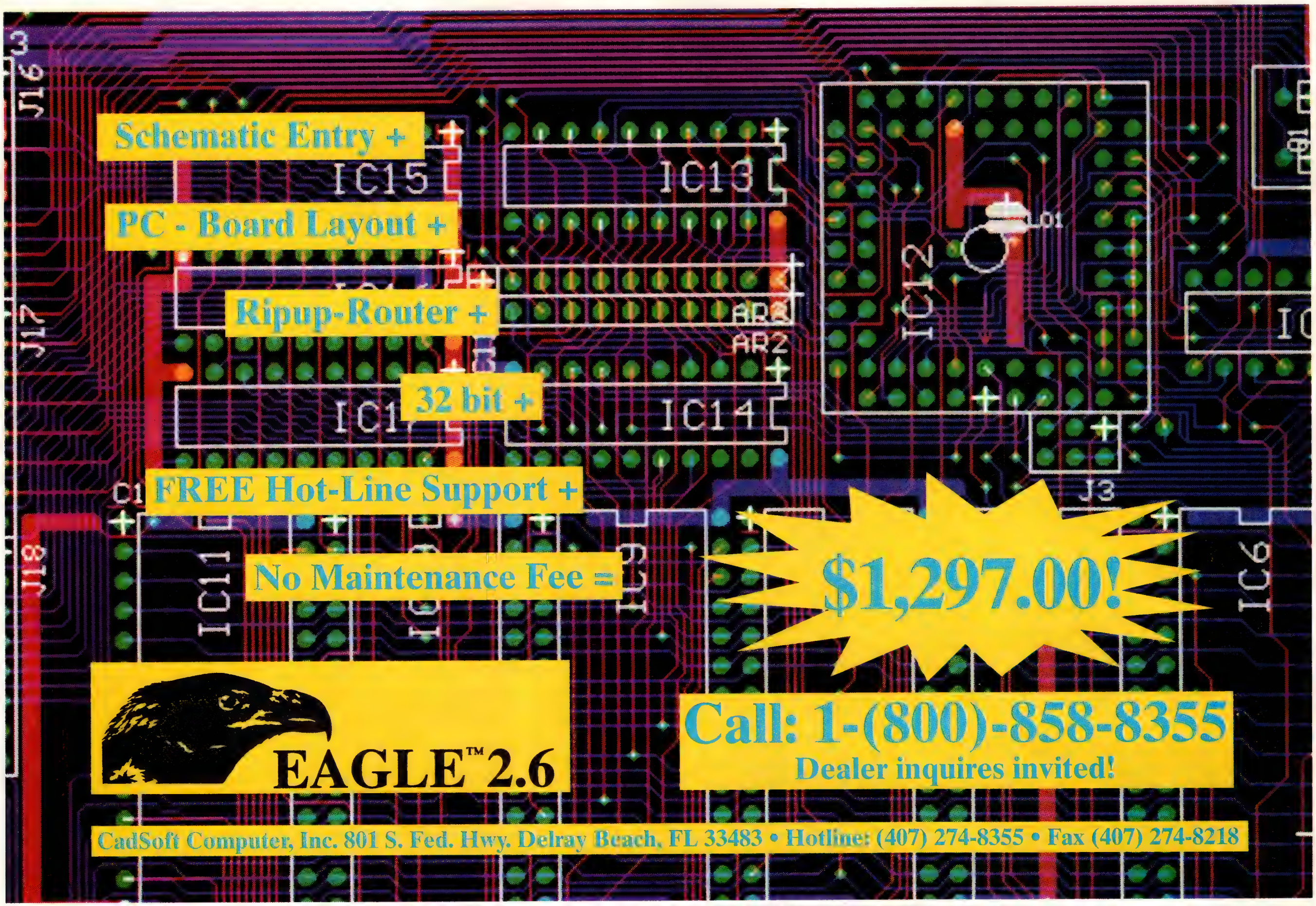

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PRODUCTS NEWSLETTER

SERVOWRITER HANDLES HYBRID SERVOS

Hybrid servo techniques have become the popular choice for small, high-capacity hard-disk drives because the servo positioning is very precise. Hybrid servo systems combine dedicated surface and embedded servo technologies within a drive to take the benefits of each. Now, there's a servowriter that can handle drives with the hybrid servos. The HS-9000 accepts any disk size, including those under the 2.5-in. form factor. The drive is held in a customized fixture that's aligned to a laser beam. The servowriter comes with ISA and EISA bus controllers, user-configurable software, and a laser interferometer positioning system. Operator control is handled through a keypad and a color display. Available now, the HS-9000 servowriter starts at $40,000. *RNT* **CIRCLE 610**

MATLAB PORTED TO MORE PLATFORMS

Engineers working in image processing and designing neural networks and control systems must visualize and explore data and mathematical models as well as to prototype, analyze, and optimize system designs and algortithms. MathWorks MATLAB version 4.0 technical-computing software offers object-oriented graphics, sparse matrix support, sound output, and graphical user-interface controls. It runs on most workstation platforms, including Sun Solaris, DEC Ultrix, and Alpha/AXP Systems. The Natick, Mass., company has quantity and educational dicounts for MATLAB software, which starts at $2995 for a single-seat workstation license; (508) 653-1415. *SVT* **CIRCLE 611**

TOOLSET SYNCHRONIZES SOURCE WITH DESIGN

Combining the tools in Smartsystem 2.0 from Procase Corp., San Jose, Calif., with the C Development Environment from IDE, San Francisco, gives developers an interactive environment for forward and reverse engineering of C source code. This ensures that their source code stays in sync with their front-end designs. The integration enables developers to use IDE tools for initial design, use Smartsystem during coding or maintenance, and when code is complete, use the integration to automatically generate as-built documentation in the form of program structure and data-structure diagrams in the IDE design tools. Many companies have existing code for which no design documentation exists—the integration can be used to automatically reverse engineer the code and generate up-to-date documentation within IDE. Call (408) 433-9500. *SVT* **CIRCLE 612**

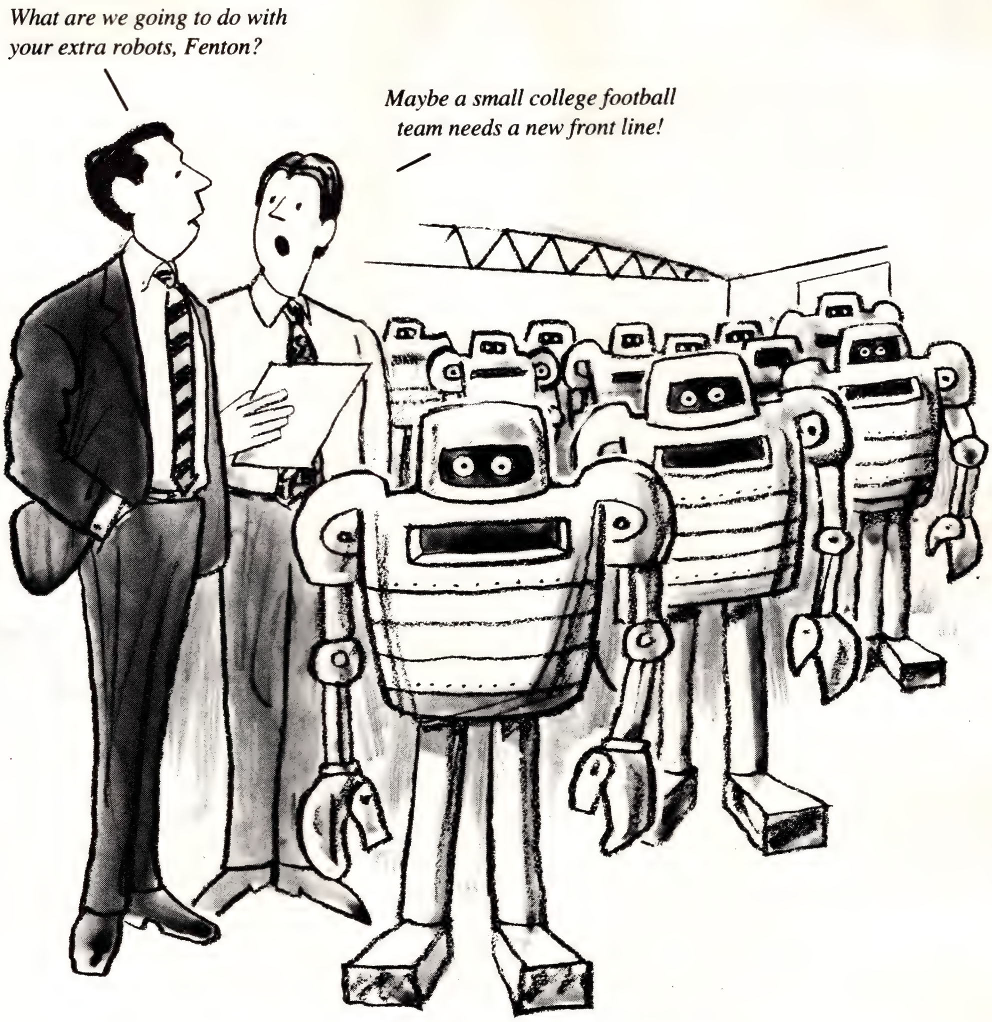
ICs CONNECT PCI TO SCSI OR IDE DEVICES

SCSI or IDE devices can be connected to a PCI local bus with a family of integrated interface ICs. The AIC-7850 and 7870 SCSI host-adapter chips, from Adaptec, Milpitas, Calif., handles data rates of 10 and 20 Mbytes/s, respectively, making it possible for them to exploit the 133-Mbyte/s speed of the PCI bus. Each chip is built with the company's PhaseEngine RISC processor. The two single-chip solutions connect directly to a motherboard or add-in card and require no additional logic. In large quantities, the 7850 and 7870 will cost $25 and $39, respectively. For IDE-to-PCI connection, the AIC-25PC10 features a 20-Mbyte/s transfer rate. This part is suited for high-speed disk drives that were limited by the slower transfer rate of the IDE connection. Extensive software support is available for all three ICs to accelerate product development. Available now, the 25PC10 costs $6 to $8 each in large volumes. Call (408) 945-8600. *RN* **CIRCLE 613**

CACHE SRAMs SUIT PENTIUM NEEDS

System designers looking for high-speed SRAM performance in very deep or wide cache configurations, but without the performance degradation common to large cache arrays and high clock speeds, will be heartened by the ChipFrame application-specific cache SRAMs from MicroModule Systems (MMS), Cupertino, Calif. These memory products are designed to support leading-edge microprocessor-based applications with clock rates of 66 MHz or greater. Designs are available with burst-control pins capable of supporting the Intel i486 and Pentium burst sequence. Motorola MC 68040-specific configurations are also available, as are designs tailored for RISC processors, such as DEC's Alpha AXP, Sun Microsystems's Sparc, HP's PA-RISC, MIPS's R4400, and other RISC architectures. The caches are based on MMS's ChipFrame MCM-D technology, which offers high functionality in less real estate than either discrete ICs or MCM-L solutions. Call (408) 864-7437 for pricing and delivery. *DM* **CIRCLE614**

Edited by Clifford Meth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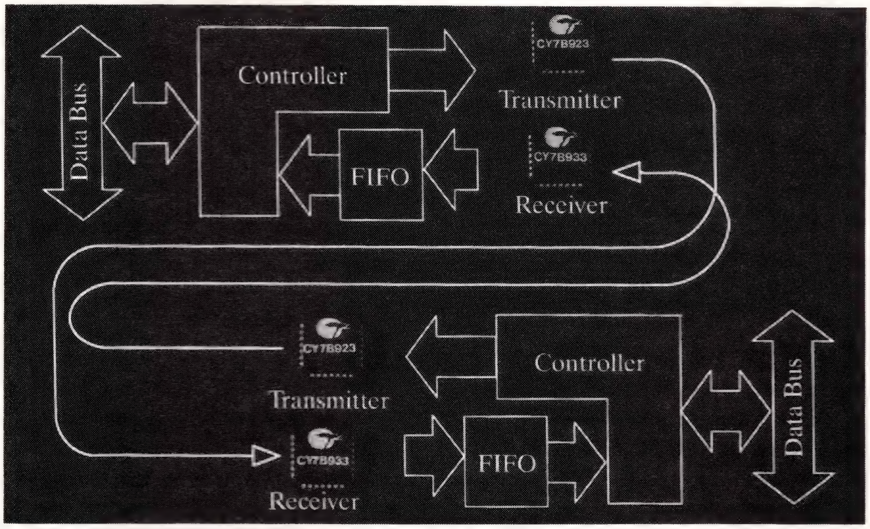


The industry's first high-speed, point-to-point serial communications chip set made using biCMOS process technology for fast data transfer and low power consumption, HOTLink (High-speed Optical Transceiver Link) is Cypress Semiconductor's first entry into the erupting data-communications market. The company's new devices provide extremely high-speed communications—160 to 330 Mbits/s—for a number of emerging applications, such as the Fibre Channel, Asynchronous Transfer Mode (ATM) networks, the Enterprise System Connection (ESCON), serial backplanes, and military applications.

HOTLink is a flexible, point-to-point building block. It can be used for data transfer in applications such as disk-to-peripheral, server-to-server, generic serial bus/backplane, and video-imaging communications. HOTLink has an 8-bit parallel port and transmits over high-speed serial links, including fiber, coaxial cable, and twisted pairs. The chip set includes the CY7B923 transmitter and the CY7B933 receiver. Cypress also offers the CY9266 evaluation board (which is IBM OLC-266 compatible) with fiber, coax, and twisted-pair media interfaces for simplified applications development.

The chip set, which operates from a single +5-V power supply, also offers a number of technological advances over other data-communications solutions. HOTLink chips are made using a 0.8-μm biCMOS process. According to the company, this offers power savings of at least 25% over competitive products, which utilize higher-power-dissipation bipolar or gallium-arsenide technologies to achieve similar data rates. HOTLink dissipates 350 and 600 mW for the transmitter and receiver, respectively. The product includes 8B/10B encoding (as specified in the Fibre Channel standard) and allows for a 10-bit unencoded mode, so users have flexibility to develop their own off-chip encoding solutions.

In normal operation, the transmitter can operate in either of two modes: an encoded mode and a bypass mode. In the former mode, a user can send and receive 8 bits of data and control information without first converting it to transmission characters. The bypass mode is used for systems in which encoding and decoding are performed by an external protocol controller.

In addition, HOTLink offers three 100K Pseudo ECL (PECL) outputs for point-to-multi-point applications. The chip set incorporates a completely integrated phase-locked-loop (PLL) clock synchronizer, which eliminates the need for external capacitors and resistors. It also offers a built-in self-test to allow loop-back and link-integrity diagnostics.

Eight bits of user data or protocol information are loaded into the HOTLink transmitter and are encoded. Serial data is next shifted out of the three differential PECL serial ports at the bit rate (which is ten times the byte rate).

The HOTLink receiver accepts the serial bit stream at its differential line receiver inputs, and using a completely integrated PLL clock synchronizer recovers the timing information necessary for data reconstruction. The bit stream is deserialized, decoded, and checked for transmission errors. The recovered byte is presented in parallel form to the receiving host computer along with a byte-rate clock.

The 8B/10B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. I/O ports are available to create a seamless interface with both asynchronous FIFO buffers (i.e., the CY7C42X) and clocked FIFO buffers (i.e, the CY7C44X). A built-in self-test pattern generator and checker makes it possible to test the transmitter, receiver, and the connecting link as a part of a total system diagnostic check.

Systems are migrating from parallel data transmission to serial interfaces to reduce connector size and to extend data transfer distance and speed. Consequently, HOTLink was created to reduce communications bottlenecks caused by the high volumes of data traffic found in today's applications. Emerging serial standards provide transmission speeds over 150 Mbits/s.

HOTLink is available now in production quantities. It comes in 28-pin PLCC, SOIC, and LCC packages. The HOTLink chip set (CY7B923 transmitter and CY7B933 receiver) is priced at $60 in lots of 100. The HOTLink evaluation board costs $495 each.

Cypress Semiconductor, 3901 N. First St., San Jose, CA 95134-1599; (408) 943-2600. **CIRCLE 640**

CUTTER SPEEDS ACCESS TO BURIED PROBE POINTS

The IDS P2X (ProbePoint eXtension) allows operators to perform real-time probe point cutting for debug of complex multilayer devices. The focused ion-beam (FIB) based system works with a mechanical or e-beam prober to provide interactive debug capability. Thus operators can cut probe points to gain access to buried layers without having to go off line.

The result is much faster debug and greater productivity. The key to the system is the integration of four elements: a quick-change vacuum system, a kinematic load module, CAD Layout Overlay software, and Optimal Probe Point Placement (OP^3) software.

The IDS P2X vacuum system improves the speed with which the chip can be moved from the prober to the FIB and back. Meanwhile, the kinematic mounts eliminate device alignment errors. The mounts use three rigid mounting points that exactly define both a plane and a specific position within that plane. As a result, the load module can be repeatedly returned to exactly the same position, within a couple of microns.

The CAD Layout Overlay software superimposes an outline form of the top-metal CAD layers on the FIB image. This enables the user to automatically perform an accurate local overlay alignment using the visible surface topography from the top layer and to accurately position the CAD layers that show invisible buried conductors.

The OP^3 software uses knowledge of both e-beam measurement (including the limit of an e-beam's ability to make capacitively coupled measurements on conductors buried under dielectric) and FIB modifications. The software then selects the best chip location to either measure directly or create a probe point.

The IDS P2X has an average price between $400,000 and $600,000, with delivery within 30 to 90 days, depending on the tester being used.

Schlumberger Technologies *ATE Div., 1601 Technology Dr., San Jose, CA 95110-1397; (408) 437-5091.* **CIRCLE 641**

■ *JOHN NOVELLINO*

TESTABILITY SOFTWARE EASES BOUNDARY-SCAN PROGRAMMING TASK

Version 2.0 of the Advanced Support System for Emulation and Test (Asset) incorporates advanced object-oriented programming techniques, making it easier to use, readily expandable, and portable. Asset, which helps designers debug and verify complex integrated circuits, board designs, and systems, runs under the Microsoft Windows graphical user interface and supports the IEEE-1149.1 boundary-scan standard.

Two Asset modules, the Test Vector Development System and the Diagnostic System, form the foundation of Release 2.0. The Test Vector Development System supports several ways of developing and applying test stimulus to the unit under test (UUT). The use of predefined macros eliminates the need to know the C or C++ programming languages. The system features automatic test pattern generation for the scan path and can import serial or parallel test vectors. An optional Scan Function Library eases sophisticated test programming and supports C or C++ compilers from Borland and Zortech.

The Asset Diagnostic System includes an interactive debugger and scan analyzer. The debugger permits hierarchical viewing, and access and control of device test registers within the UUT. Users can interact at a functional level by scanning instructions or data into the device's test registers and observing the results. The scan analysis module replicates many features of a logic analyzer, including waveforms and state-table displays.

Once test vectors have been developed, Scan Engine can be used to easily embed test procedures for go/no-go testing. Scan Engine works with the SN74ACT8990 test bus controller to automatically read scan vectors from the system's memory and apply them to the boundary-scan chain. The software and controller support built-in self-test and interconnect, functional, device, and logic-cluster testing.

The Test Vector Development System costs $8495, the Asset Diagnostic System $13,995, the Scan Function Library for C++ $2495, and Scan Engine $12,000 plus royalties.

Texas Instruments Inc., *Literature Response Center, P. O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 3804.* **CIRCLE 642**

■ *JOHN NOVELLINO*

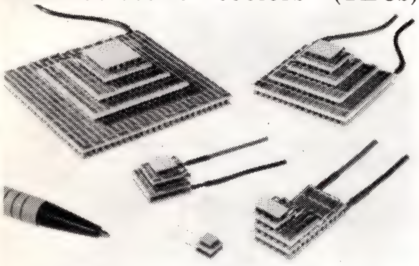
TEST SOFTWARE ENSURES FULL-CHIP ASIC TEST

Two ASIC test tools allow designers to address the various test strategies used for the chips within a consistent design-for-test environment. Test Manager lets designers automatically explore and select the best test methods for individual chip modules and to achieve cumulative fault coverage for the entire chip. This multi-style, multi-pass testing technique allows a design to use several test methodologies with different protocols. Methods covered include full scan, constraint-based partial scan, boundary scan, functional vectors, and user-defined test structures. The TestSim fault simulator, which is fully integrated with Test Manager and other Synopsis logic and synthesis tools, leverages existing designs by accepting their associated functional vectors for automatic test pattern generation. The simulator is supported by more than 100 existing certified ASIC vendor libraries. Test Manager will be included in Version 3.1 Test Compiler and Test Compiler Plus at no extra charge. TestSim is expected to cost $35,000. The products will be available in the first quarter of 1994. JN

Synopsis Inc., 700 E. Middlefield Rd., Mountain View, CA 94043-4033; (415) 694-4255. **CIRCLE 643**

CASCADED COOLERS INCREASE CAPACITY

A broad range of multistage thermoelectric cascades features a series of thermoelectric coolers (TECs) stacked or cascaded atop one another for increased temperature differentials compared with standard, single-stage TECs. From two to six stacked TECs can be supplied for cooling differentials of up to 131°C. A total of 24 standard cascade configurations are available ranging from a two-stage model rated at 2 A with a temperature differential of 91°C to a six-stage version rated at 3 A. Typical pricing for a two-stage cascade in lots of 100 is $50.75. Delivery is in four to six weeks. DM



MELCOR, 1040 Spruce St., Trenton, NJ 08648; Dick Duenn, (609) 393-4178. **CIRCLE 644**

UHF TRANSISTORS HANDLE TUNER AGC

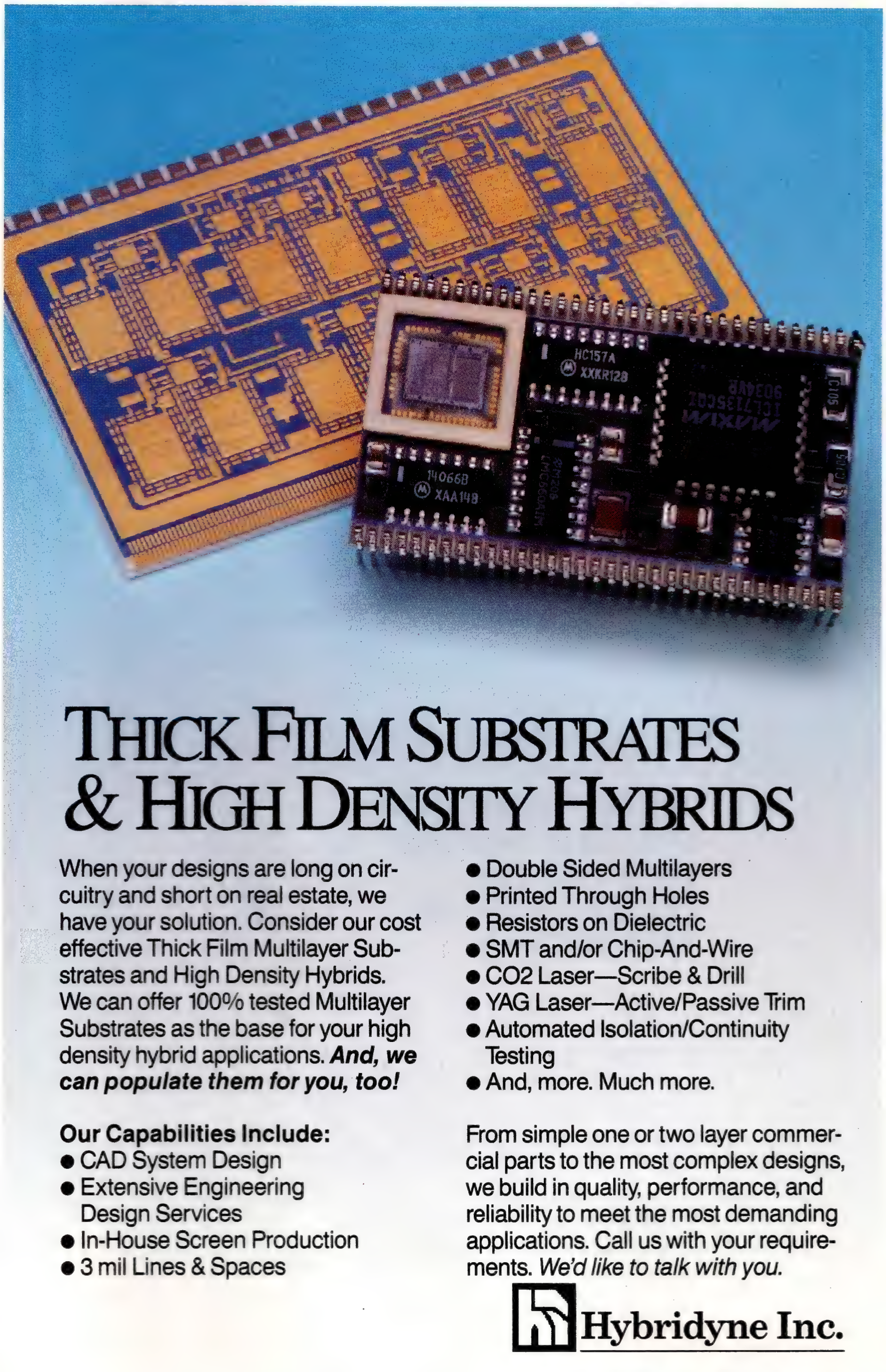
Two dual-gate MOSFETs are available for use in the automatic-gain-control stages of VHF and UHF tuners. The BF908, which operates from a 12-V tuner supply, has the high transfer admittance, low input capacitance, and superior cross-modulation performance needed for low-noise, high-gain RF amplification. The BF904 offers similar advantages while being the world's first MOSFET for tuners that operate from a 5-V supply. In addition, the BF904 includes an internal bias circuit to reduce cross modulation and eliminate up to four external bias components. Its internal biasing cuts component counts. Call for pricing and delivery. DM

Philips Components, Discrete Products Div., P.O. Box 10330, Riviera Beach, FL 33404; (800) 447-3762. **CIRCLE 645**

SILICON PHOTODIODE DETECTS LOW LEVELS

A general-purpose light detector for both high and low levels of illumination is available in the BPW34 silicon photodiode. The unit detects modulated light at frequencies up to 10 MHz. Its active area measures 7.1 mm^2 and the unit is housed in a small plastic DIP. Call for pricing and delivery information. DM

Centronic Inc., 2088 Anchor Ct., Anchor Business Park, Newbury Park, CA 91320; (805) 499-5902. **CIRCLE 646**



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SWITCHING 8 A AT 500 V, P-CHANNEL IGBT REPLACES N-CHANNEL PAIR

Until now, if you wanted to build a high-voltage high-current half bridge for power control, you had to use a pair of n-channel MOSFETs, or a pair of their siblings—the IGBT. Both require complex drive circuitry (such as charge pumps or boot-strap circuits) to pull the gate of the high-side n-channel switch 10 to 15 V higher than the bridge's supply. But Harris has come up with a 500-V, p-channel IGBT rated at maximum continuous currents of 12 A at 25°C and 8 A at 90°C. The HGTD8P50G1's maximum forward-voltage drop (the collector-emitter saturation voltage) runs just 3.7 V while passing 8 A. And it comes in the miniature TO-251 (with leads) and TO-252 (surface-mounted) plastic power packages.

When a p-channel IGBT replaces the high-side n-channel switch, the power half-bridge works just like a low power CMOS inverter. The gates of both devices are tied together. Thus, a positive-going pulse turns the low-side switch on and the high-side switch off, and the output goes low. Returning the gates to zero volts turns the high-side switch on, the low-side switch off, and the output of the bridge goes to the supply rail.

The p-channel IGBT is also a natural as a stand-alone high-side switch driving loads, which must be connected to ground. That is, the IGBT is connected between the positive supply rail and the load. In this configuration a short to ground does not damage the load. Like the half-bridge, an n-channel high-side switch requires a charge pump or bootstrap circuit to turn the device on.

In lots of 1000, the TO-251 packaged 500-V IGBT (HGTD8P50G1) costs $1.44 each, its surface-mount cohort in the TO252 (HGTD-8P50G1S) goes for $1.45 each in similar quantities.

Harris Semiconductor, *P.O. Box 883, Melbourne, FL 32901; 1-800-4-HARRIS, ext. 7122.*
CIRCLE 647

■ *FRANK GOODENOUGH*

DENSE CONVERTER SERVES PULSE TASKS

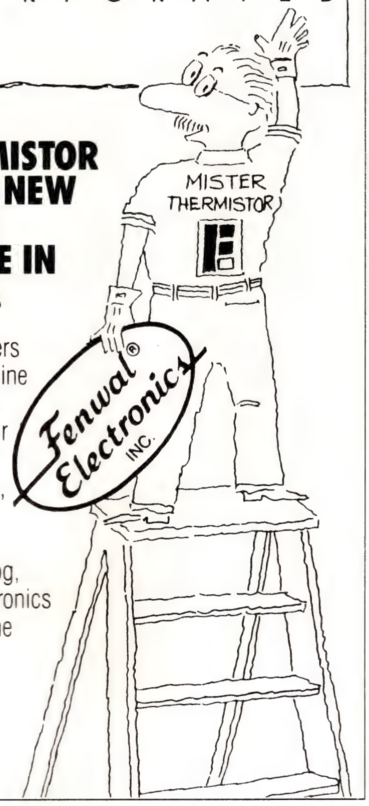
A single-output power supply for pulse-power applications features active current-sharing circuitry for N+1 parallel operation. The ac-dc or dc-dc units accept either 115-V ac, three-phase or 270 V dc inputs and provide up to 1000 W of output power at from 12 to 48 V dc. Other features include overcurrent and overvoltage protection, full input-to-output isolation, synchronization, and excellent dynamic-load response. Pricing varies with configuration. DM

Lambda Novatronics Inc., 500 S.W. 12th Ave., P.O. Box 878, Pompano Beach, FL 33061-0878; (305) 942-5200. **CIRCLE 648**

5-TO-3-V CONVERTERS BOOST CURRENT RANGE

An upgrade to the EZ-Dropper line of 5-V-to-3-V dc-dc converters provides a wider current range than does the original design. In addition, a low-current version has been added to further simplify the generation of 3 V from 5-V power rails. The low-current device offers a current range of 5 to 250 mA. For the balance of the line, the low-current rating has also been dropped to 10 mA from the previous low of 200 mA. The rated high-current output remains 1 A. Redesignated the EZ5Z3 from the former SC5Z3, the linear, noise-free parts generate no EMI or voltage spikes inherent to switching converters. The lower-current ratings are intended to aid designers of boards with long traces. Pricing for the EZ5Z3L family is $1.86 in 100s. DM

Semtech Corp., 652 Mitchell Rd., Newbury Park, CA 91320; Art Fury, (805) 498-2111. **CIRCLE 649**



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HOST ADAPTERS CONNECT SCSI TO ALMOST ANY STANDARD BUS

Peripherals built with a SCSI interface offer the promise of higher performance because the data-transfer rates of SCSI are higher than those of the alternatives, such as an IDE interface, or serial or parallel ports. Now, thanks to the developments of QLogic Corp., even higher performance can be achieved by connecting the SCSI peripheral to almost any standard computer bus.

The QLA400 family of SCSI host adapters is available in four different versions. It can connect to an ISA bus (QLA400-IA), an EISA bus (QLA400-EA), a VL-Bus (QLA400-VL), or a PCMCIA slot. The PCMCIA version, the QLA400-PA, fits in a Type-2 card slot. In addition, the QLA-1000 supplies a connection to the PCI local bus.

The QLA400 family is based on the company's ESP406, a single-chip high-performance SCSI processor that automates the performance of SCSI operations at hardware speed without any host CPU intervention. The boards, compatible with most SCSI standards, are supported by software drivers for DOS, Windows, Windows NT, Novell NetWare, SCO Unix, and OS/2.

The PCI-based board features a burst transfer rate of 132 Mbytes/s and a sustained rate of 20 Mbytes/s. It can process 2000 I/O requests/s while queuing an additional 1600 requests/s. Evaluation units of the QLA-1000 are available now. Production quantities will come in January. Evaluation prices for the QLA400-IA, QLA400-EA, QLA400-VL, and QLA400-PA are $121.40, $215.90, $206.40, and $210, respectively. All come with documentation, software drivers, and installation software. Substantial discounts for large lots.

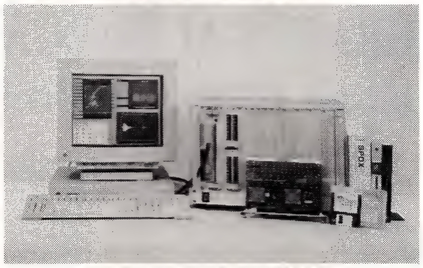
__QLogic Corp.,__ 3545 Harbor Blvd., P.O. Box 5001, Costa Mesa, CA 92628; (800) 662-4471 or (714) 438-2200. **CIRCLE 650**

■ *RICHARD NASS*

HARDWARE/SOFTWARE CONNECT VME DSP BOARD TO SPARCSTATION

The Hydra DSP board from Ariel Corp., Highland Park, N.J., can now be linked to Sun Sparcstations with the HydraLink hardware and software. Hydra is a 200-MFLOPS board built with up to four Texas Instruments 320C40 processors. HydraLink was developed by ESI Computing. It consists of a five- or twelve-slot card cage, one or more VMEbus-based Hydra boards, an SBus-to-VMEbus adapter, and SunOS device drivers. The card cage is available in either tabletop or rack-mounted versions, and can be located up to 20 ft. from the SparcStation.

DSP code can be written and debugged on the Sparcstation, then downloaded to the Hydra board. There's enough throughput to use the SparcStation for display purposes. The bus-interface hardware translates the address maps between the SBus and the VMEbus at a transfer rate of up to 10 Mbytes/s. Both SBus and VMEbus masters can access their respective VMEbus and SBus slaves without affecting any current bus activity.



HydraLink sells for $12,490. Software support, including cross- and co-development tools and run-time software, is also available. The Hydra DSP board is available directly from Ariel.

__ESI Computing Inc.,__ 468 Westford Rd., Carlisle, MA 01741; (508) 369-8499. **CIRCLE 651**

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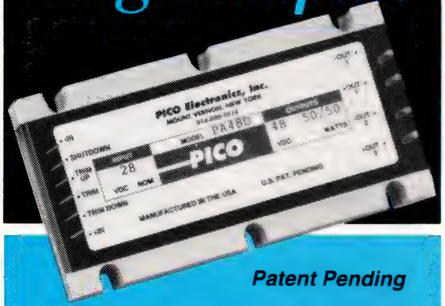

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STATE-DIAGRAM WINDOWS SOFTWARE INCLUDES CONCURRENCY

Making it easier to design state machines, the software tool Better State makes it possible for state diagrams to include factors such as concurrency and hierarchy, while retaining the intuitive and visual appeal of state diagrams. Developed by R-Active Concepts, the program runs under the popular Microsoft Windows 3.x graphical user interface on IBM PCs and compatibles. With the software, users can create graphical images of state diagrams on one or more linked pages, annotate them, and then generate either VHDL, Verilog, or C-code to implement the state functions.

Such features make it much easier to create state descriptions for reactive control systems. Reactive systems have inputs (or outputs) that continuously and endlessly arrive (or are sent to) a plurality of partially correlated entities in the environment. For example, a telephone answering machine never has its inputs ready; inputs arrive continuously and endlessly, in a non-deterministic order (the order of the inputs is not known in advance).

In Better State, users can draw states, edges, illustrate threads of concurrent control, and annotate the diagrams. VHDL or Verilog can be used to annotate the diagrams, thus enabling the code in the diagram to refer to code written elsewhere. The windows also provide a visual page structure diagram that allows the user to comprehend and access all portions of the diagram with a mouse click. Smart graphics make it easy to manipulate the diagrams—when moving a state, all connected edges and text move with it. And to avoid a cluttered look, text can be hidden. Templates supplied with the software enable users to schedule the design deterministically, stochastically, or using specific scheduling algorithms (for example, round robin, and so forth).

A single-user version of Better State sells for $690. The software is available now.

R-Active Concepts, *20654 Gardenside Circle, Cupertino, CA 95014; Doron Drusinsky, (408) 252-2808.* **CIRCLE 652**

■ *DAVE BURSKY*

GRAPHICAL DATA-ANALYSIS SOFTWARE RUNS UNDER WINDOWS

A Microsoft Windows version of DADiSP graphical data analysis software extends the capabilities of the software, which collects, analyzes, and displays scientific and technical data. DADiSP/32-WIN is compatible with previous versions, so that existing worksheets, datasets, macros, and command files operate without change. The software combines hundreds of built-in functions to perform graphical data analysis, mathematical and statistical analysis, data management, and FFT analysis.

As a Windows application, DADiSP/32-WIN can run multiple applications, import data by means of the Notepad Utility, switch between DADiSP and other programs, and dynamically resize DSDisp application windows. The software also automates DAPiSP worksheets for background operation, performs clipboard cut and paste, manages memory allocation, and uses Windows printer drivers.

Other new features are icon buttons for session control and data manipulation, QR and SVD matrix decomposition, Sobel edge detection, minimum, median, and maximum image filtering, time and date stamping, as well as string manipulation and data type conversion. Price depends on configuration.

DSP Development Corp., *One Kendall Square, Cambridge, MA 02139; (617) 577-1133; fax (617) 577-8211.* **CIRCLE 653**

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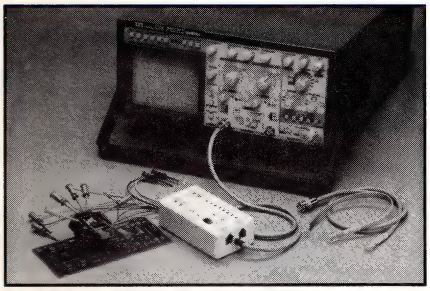

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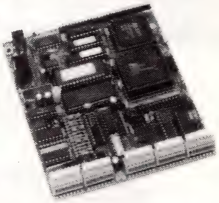

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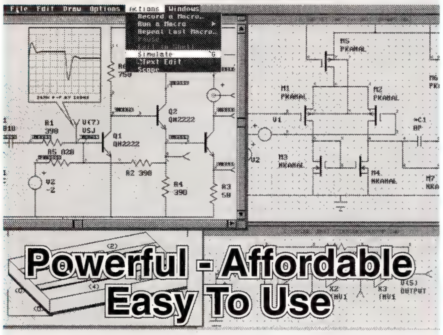

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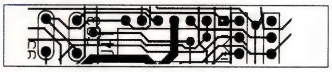

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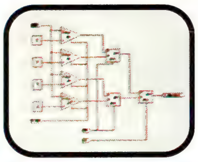

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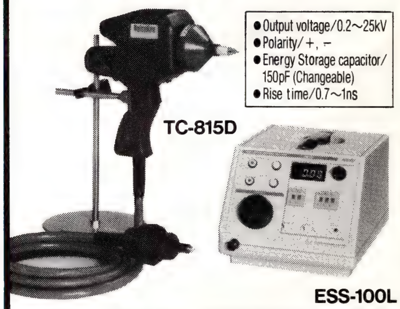

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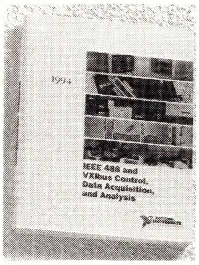


The 1994 catalog from National Instruments, Austin, Texas, was redesigned to make it easier for designers to find technical specifications. The 528-page, full-color catalog describes software and hardware products for developing integrated measurement and instrumentation systems based on the IBM PC/XT/AT, PS/2, EISA, Macintosh, Sun, Hewlett-Packard, DEC, and other computer platforms. Five color-coded sections cover instrumentation software, GPIB, data acquisition, VXI/MXI, and customer education. The product sections feature comprehensive tutorials, including application examples. JN

CIRCLE 781

GUIDE DETAILS MODULAR PRODUCTS

White Technology's *Modular Product Guide* contains production descriptions and specifications for the Phoenix, Ariz., company's static RAMs, EEPROMs, flash PROMs, and microcontrollers. Military screening is available to meet various mil standards. The facility is certified to MIL-STD-1772B. For the free guide, contact (602) 437-1520; fax -9120. SVT **CIRCLE 782**

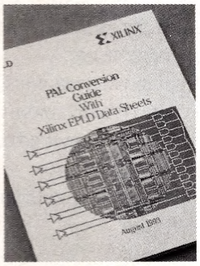
WIRELESS TEST PRODUCTS

A new brochure describing over 30 products for wireless communications test (literature 5091-7273) is available for free from Hewlett-Packard, Palo Alto, Calif. The 18-page, full-color brochure is designed to help communications managers and engineers select HP test products for research and development, manufacturing, and field test. It includes a table that shows the communications systems that can be tested and the types of measurements that can be made. Call 800-452-4844. CM **CIRCLE 783**

BOOK DETAILS CARE OF TOKEN RING LANS

"The Token Ring Healthcare Guide" is a 48-page reference book for checking, documenting, and evaluating token-ring local-area networks. The book, which is offered for free by Fluke Corp., Everett, Wash., provides step-by-step guidelines for solving the most common network problems. The first two sections of the book are called "Preventing Problems" and "Solving problems." These are followed by appendices on token-ring errors, operation, troubleshooting, and cable testing. Also included is a glossary of local-area network terms. Contact Fluke at (800) 443-5853. JN **CIRCLE 784**

PAL CONVERSION GUIDE OFFERED



The PAL Conversion Guide from Xilinx, San Jose, Calif., demonstrates the ease of programmable array logic conversion with the company's EPLDs. The guide contains a PAL conversion application note, data sheets, and information of compilers and languages. Call the 24-hour literature hotline for a copy (800) 231-3386. SVT **CIRCLE 785**

COMPUTER INSTRUMENT PRODUCTS DESCRIBED

A wide range of software and hardware products for computer-based integrated measurement and instrumentation systems is described in a 528-page, color catalog from National Instruments Corp., Austin, Texas. Included are products for the PC/XT/AT, PS/2, EISA, Macintosh, Sun, Hewlett-Packard, and DEC. The catalog is color-coded into five sections: Instrumentation Software, GPIB, Data Acquisition, VXI/MXI, and Customer Education. Complete ordering, pricing, and warranty information is included. JN **CIRCLE 786**

FUME EXTRACTORS

The Tip-Evac Fume Extraction brochure, free from Pace Inc., Laurel, Md., illustrates a variety of fume extraction systems to remove harmful fumes from soldering operations. The brochure also explains the benefits of fume source capture by removing particulates and gases before they reach a designer's breathing zone. The Tip-Evac fume extraction systems allow users to precisely position a suction tube on the soldering iron and remove fumes as they are produced. CM **CIRCLE 787**

ELECTRONIC PARTS AND COMPONENTS

A free catalog from MCM, Centerville, Ohio, contains over 20,000 parts and components—more than 1,400 of them introduced for the first time in this publication. The categories of products include semiconductors, television parts, power supplies, telephone parts and accessories, connectors, tools, batteries, speakers, VCR parts, and test equipment. MCM has also expanded its lines of computer and cellular products. CM **CIRCLE 788**

FLEXIBLE HEATER

A brochure from Elmwood Sensors Inc., Pawtucket, R.I., describes a flexible heater sample kit to help designers specify and determine customized requirements for virtually any heater application. The kit comes with Kapton or UL-approved silicone rubber materials, with attached pressure-sensitive adhesive backings as an option. It provides 13 different shaped heaters to meet application considerations, including a version for thermostat mounting. Heaters used in combination can provide a number of resistances and wattages, especially when used in conjunction with a voltage regulator. The Elmwood Sensors Flexible Heater Sample Kit provides a materials reference guide chart, an information booklet, and other technical information such as heater-mounting suggestions for customer testing in prospective applications. CM

CIRCLE 789

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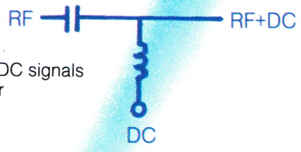

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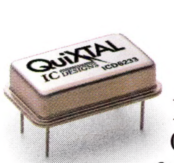

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